Reed Electronics Group

Programmable servo filters smooth motion control Page 15

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April 28, 2005
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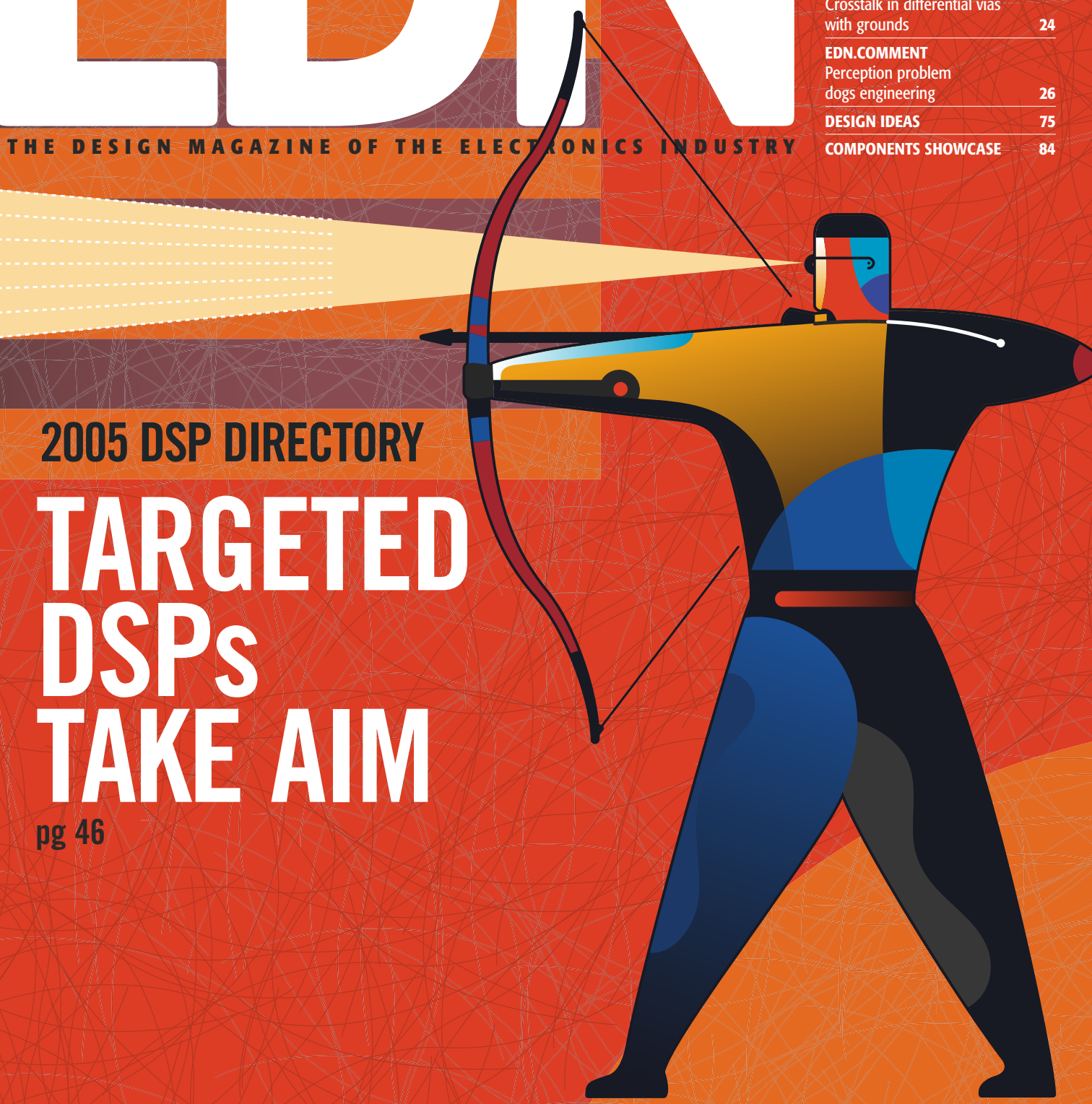

2005 DSP DIRECTORY

TARGETED DSPs TAKE AIM

pg 46

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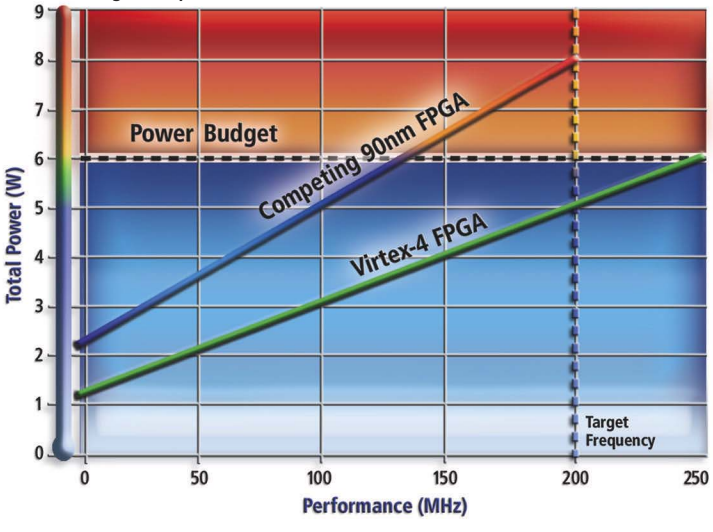

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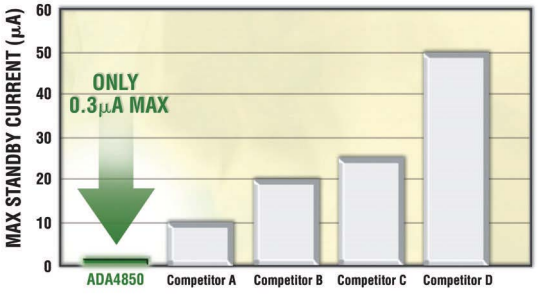

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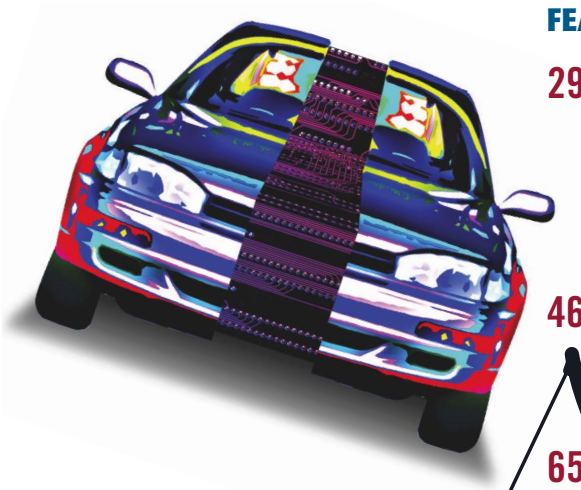
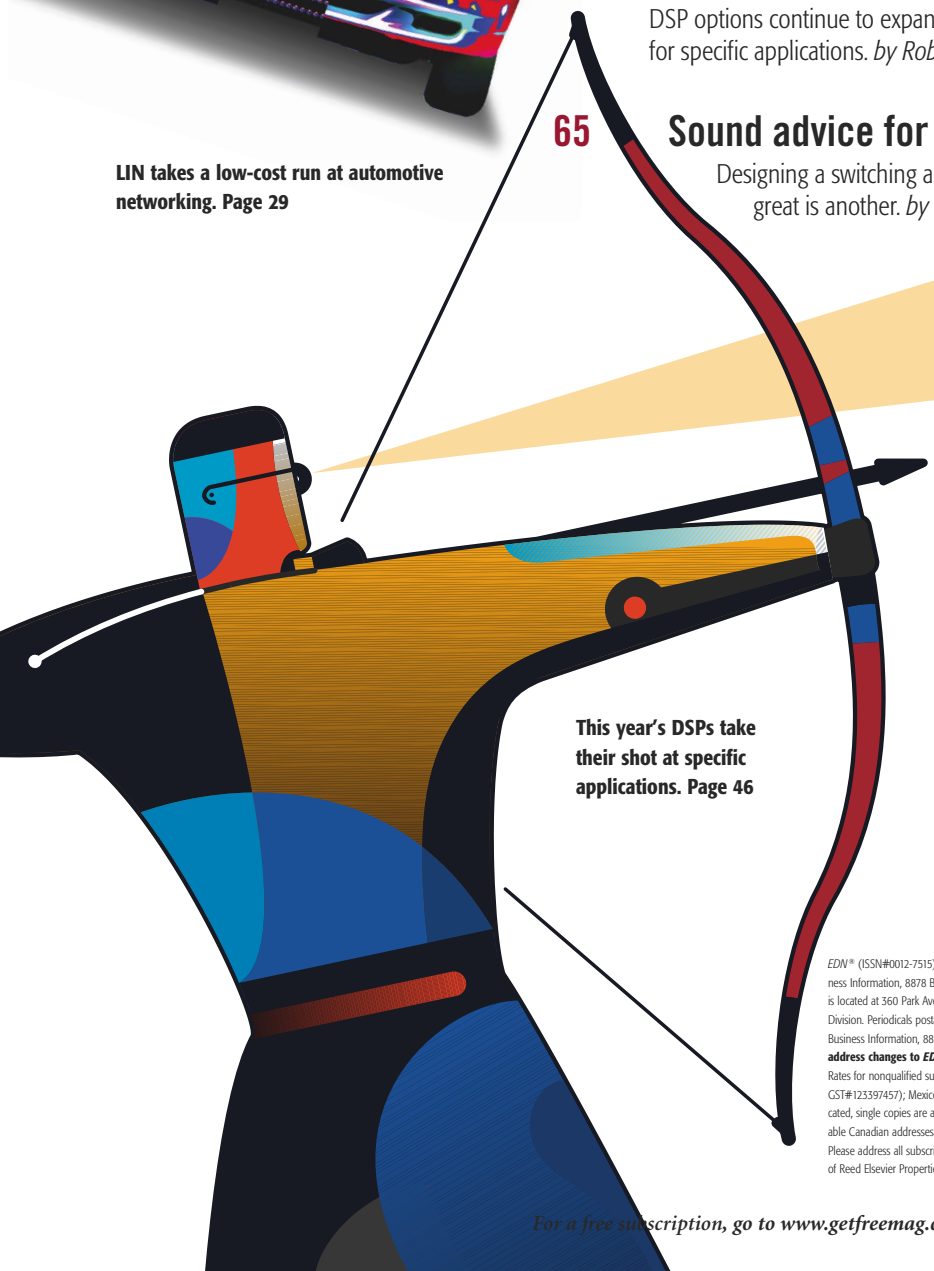


LIN takes a low-cost run at automotive networking. Page 29

FEATURES



This year's DSPs take their shot at specific applications. Page 46

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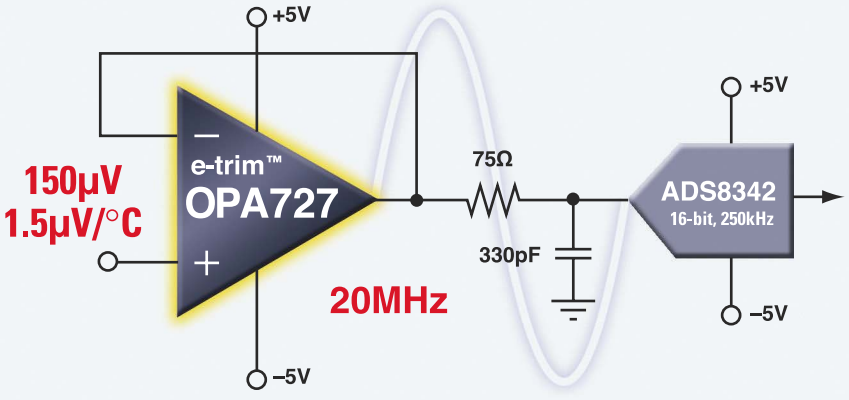
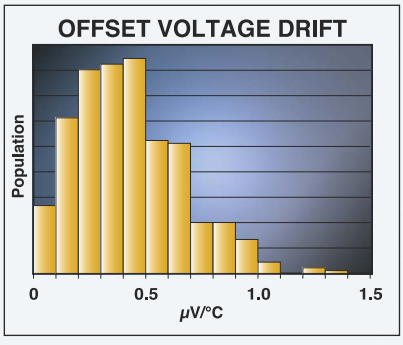
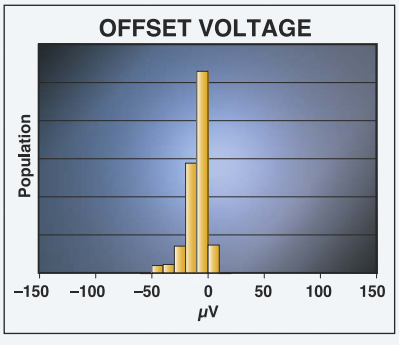
150µV max Offset, 20MHz Bandwidth

New e-trim™ Technology Offers 1.5µV/°C max Drift







Using the new **e-trim™ technology**, the OPA727 amplifiers are **calibrated** not only for offset voltage, but also for the variation of **offset voltage over temperature** — a **feature offered only by TI**.

Device	V_{OS} (µV) (max)	Drift (µV/°C) (max)	Band-width (MHz)	Slew Rate (V/µs)	Supply Voltage (V)	I_Q (mA/ch)	Smallest Package	Price Starts 1K
OPA727/28	150	1.5	20	30	4-12	4.3	DFN 3x3mm	$1.45
OPA725/26	3000	4 typ.	20	30	4-12	4.3	SOT23	$0.90

Burr-Brown Products from Texas Instruments

▸ e-trim™ Technology

- Post-packaging digital trimming
- Trimming of offset drift for best-in-class temperature stability
- Very tight offset distribution

▸ Features

- 150µV max V_{OS} offset
- 1.5V/°C max drift
- Low input current: 10pA
- Wide bandwidth: 20MHz
- Rail-to-rail output
- Wide supply range: 4V to 12V, ±2V to ±6V
- Micropackages

MSOP-8

DFN, 3x3mm

▸ Applications

- Precision ADC driver
- Photodiode amplifier
- Active filters
- Medical scanners
- Security scanners
- High-end audio
- Fluid analyzers

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Datasheets and Samples

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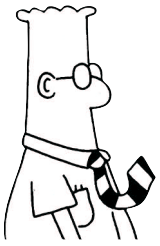

Dilbert. Page 16

Coplanar connector has low insertion loss and crosstalk. Page 84

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BLOGS

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by Maury Wright, Editor at Large
- Need 1 terabyte for movies and music?
- Video bypasses mobile networks, arrives on handsets
- More

►*www.edn.com/blog/150000015.html*

Brian's Brain
by Brian Dipert, Technical Editor
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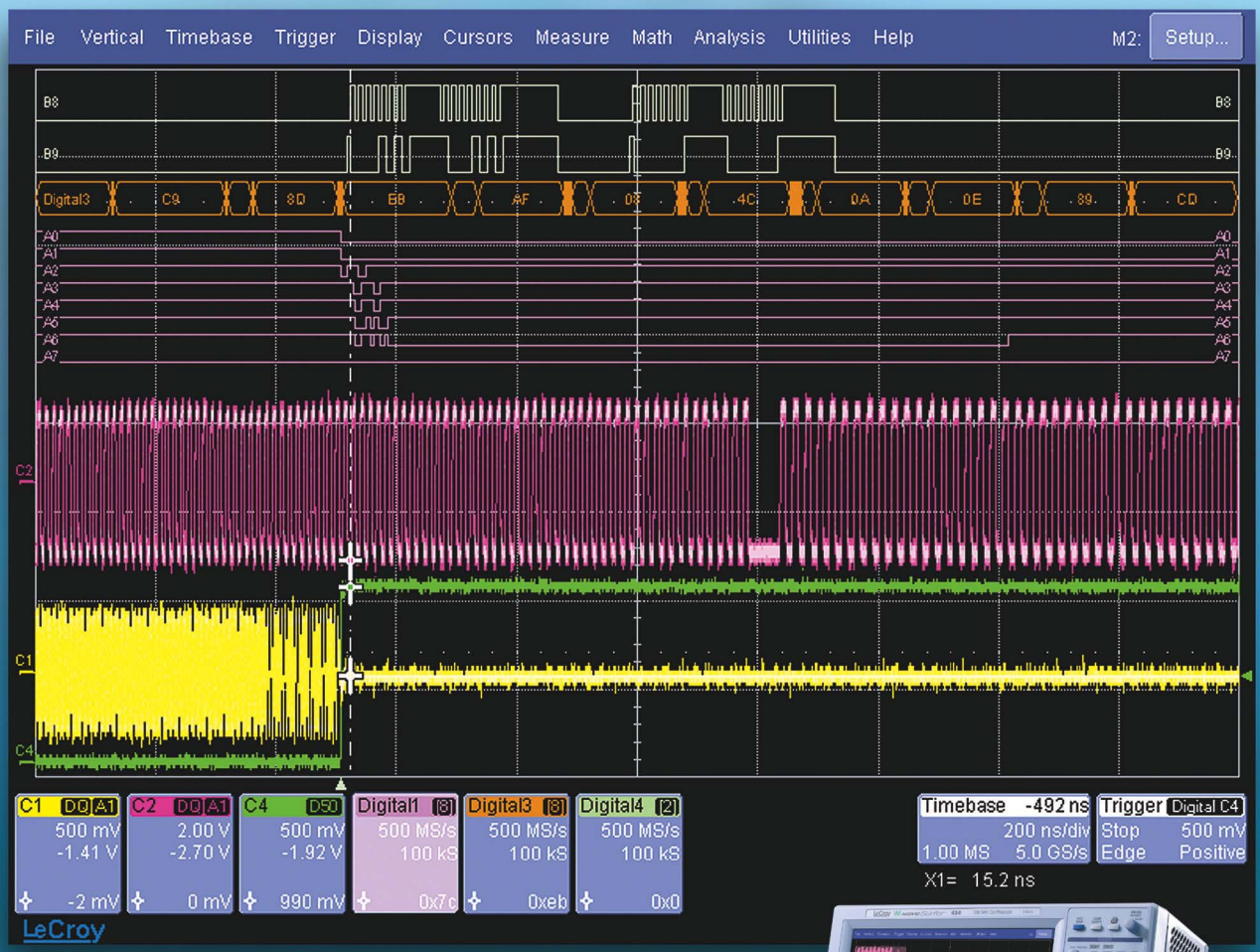

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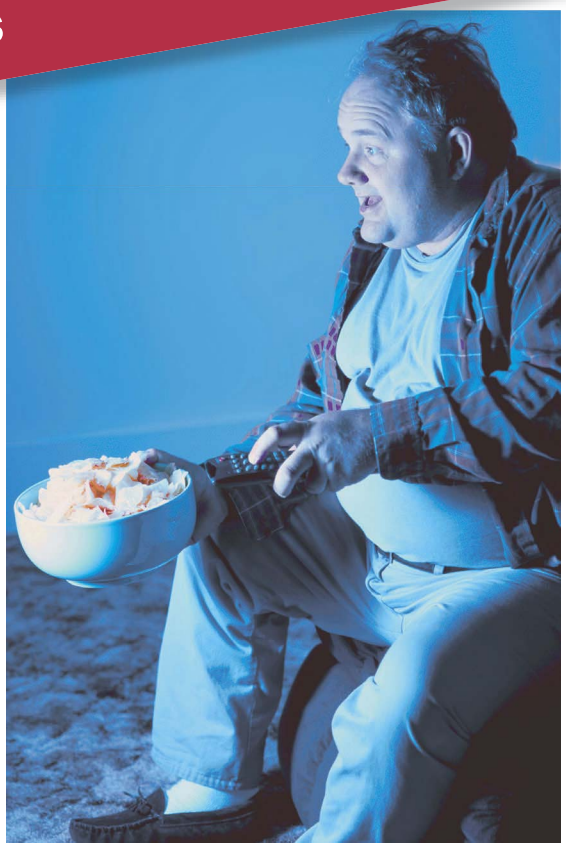

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# of Outputs	Device	Regulators PWMs	Regulators Linears	Int. FETs	V_{IN} (V)	I_{OUT} (max) (A)	Package
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3	ISL6455	1	2	✓	3.3	0.6	QFN-24
	ISL6455A	1	2	✓	5	0.6	QFN-24
	ISL6537	2	2 + Ref		2.5, 12	20	QFN-28
	ISL6532A	1	2		5, 12	20	QFN-28
	ISL6441	2	1		4.5 to 24	6	QFN-28
	ISL6443	2	1		4.5 to 24	10	QFN-28
2	ISL6227	2	0		4.5 to 24	16	SSOP-28
	ISL6440	2	0		4.5 to 24	10	QSOP-24
	ISL6539	2	0		5 to 15	8	SSOP-28
	ISL6530/1	2	Ref		5	1	SOIC-24, QFN-32
	ISL6528	1	1		3.3, 5	15	SOIC-8
	ISL6529	1	1		3.3 to 5, 12	15	SOIC-14, QFN-16

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Igor Mogilevski,
Vice President of Engineering

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For further information on the MM5 Series, and a free evaluation unit call **800-621-0733** today or go online at **www.magnetekpower.com/MM5**.

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There will only ever be one Van Drebbel.

Just like now there's only one d'Espaignet, Evans, Loukianov, Maassel, Patulea, Peterson, Schatte, and Ursu.

They all started out with the same mission: design something cool using microcontrollers from NEC Electronics. But in the end, only a select few earned the right to have their name mentioned in the same breath as Cornelius Van Drebbel. Here's to the innovations—and the innovators—that would have made Cornelius proud.

CONGRATULATIONS to the winners of the NEC Electronics microcontroller design contest.

HARDWARE CATEGORY ONE
[EV9835 board]

FIRST PLACE
Dmitrii Loukianov
Chandler, Arizona
LCR Meter

SECOND PLACE
Brian Evans
Vancouver, British Columbia
Aquarium Management Unit

THIRD PLACE
John Peterson
Menlo Park, California
NEC Tilt Handheld Game

HARDWARE CATEGORY TWO
[EV0338 & K0RE9418 boards]

FIRST PLACE
Alain d'Espaignet
Jacksonville, Florida
SmartPlanter

SECOND PLACE
Gabriel Patulea
Kanata, Ontario
Digital Audio Filter

THIRD PLACE
Alvin Schatte
Trenton, Texas
Turbine Power Meter

E-PAPER CATEGORY

FIRST PLACE
Marcel Ursu
Burnaby, British Columbia
BrainIRac

SECOND PLACE
Michael Maassel
Fargo, North Dakota
Car Stereo Tester

What makes a winner a winner? Find out at www.MadDesignContest.com/Winners

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Core memory unit of a 1954 supercomputer
—*Courtesy, The Computer History Museum*

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leading edge

What's hot in the design community

Edited by Fran Granville

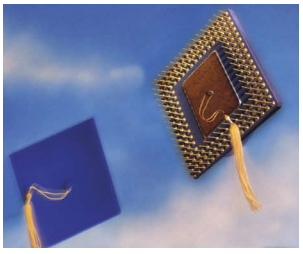


Image issue

"As long as we continue to view engineering as about widgets and not about people, we will continue to have a perception problem."

–Geoffrey Orsak, Dean, Southern Methodist University, School of Engineering, on the shortage of US engineering graduates

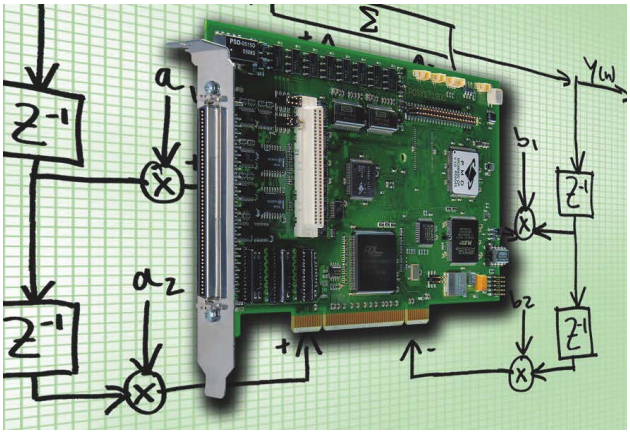
Programmable servo filters smooth motion control

By Warren Webb

Targeting medical, scientific, and general-automation applications, Performance Motion Devices recently announced the Magellan-PCI motion controller with dual biquad filters. Available in one-, two-, three-, and four-axis versions, the high-performance Magellan-PCI motion-control card supports dc brush, brushless, microstepping, and pulse and direction motors. The dual biquad filters can produce two polarities of lowpass output, as well as highpass, bandpass, and notch filters.

Additional features include trajectory generation, servo-loop closure, quadrature-signal input, motor-output signal generation, servo trace, on-the-fly changes, and commutation. The device supplies servo-loop rates as fast as 50 µsec/axis, a 5 million-count/sec quadrature-encoder-input rate, and pulse and direction output as fast as 5 million pulses/sec. The card accepts input parameters, such as position, velocity, acceleration, deceleration, and jerk, and automatically generates the programmed trajectory. Magellan-PCI prices start at $638 (OEM quantities).

▶**Performance Motion Devices**, www.pmdcorp.com.



With dual biquad filters at the output of the servo loop, the new Magellan-PCI motion controller delivers reduced resonance, faster transfers, and smoother motion.

Resistor array divides, so design conquers ratio needs

Get precision voltage division using a low-drift, close-tracking ratiometric resistive divider in a two-element SOT-23 or a three-element SOT-143 package.

The venerable resistor divider is still a staple of high-precision analog circuits, because it enables measurement architectures that depend not on absolute component values, but only on their ratios, which are more stable. BI Technologies has put a series-connected, two-resistor divider into a three-lead SOT-23 package, forming a precision voltage divider. The ultrastable resistors of the SSI series are available in standard ratios of 1-to-1, 1-to-4, and 1-to-10. Tolerances are as tight as 0.1%, and the more critical temperature coefficient is ±25 ppm/°C with tracking tolerance better than ±5 ppm/°C.

BI fabricated the resistors using nichrome thin-film technology on a silicon substrate. The device's size lets designers place it close to the circuit area of interest, thus "eliminating the need for the long traces and complex routing schemes required for large networks," according to Mike Torres, application engineer and product marketing manager for BI. The SSI series is also available with three resistors in a network in a four-lead SOT-143 package. Prices begin at 30 cents (10,000).

—by Bill Schweber

▶**BI Technologies**, www.bitechnologies.com.

Power-industry coalition announces PMBus standard, forms SIG

A coalition of power-supply and semiconductor companies led by Artesyn Technologies has released Version 1.0 of the PMBus (Power Management Bus) specification, which defines a protocol to manage power converters and a power system using communication over the SMBus digital-communication bus. The coalition has also announced the formation of an SIG (special interest group), the SM-IF (System Management Interface Forum), to further develop and promote the PMBus power operating system. The SM-IF comprises the PMBus Implementers Forum and the Smart Battery System Implementers Forum. SM-IF will also take over responsibility for the SMBus.

The SMBus is essentially compatible with the I²C bus, a popular two-wire bus that handles inter-IC control. "The I²C bus is a highly prevalent interface on embedded microprocessors; it's just all over the place," says Michael Stefani, director of product marketing for Artesyn. "SMBus adds an alert line to I²C, making it just a short step from I²C to SMBus."

In addition to Artesyn, the initial coalition comprises Astec Power and semiconductor manufacturers Intersil, Microchip Technology, Texas Instruments, Volterra Semiconductor, Summit Microelectronics, and Zilker Labs (www.astecpower.com, www.intersil.com, www.microchip.com, www.ti.com, www.volterra.com, www.summitmicro.com, www.zilkerlabs.com).

Conspicuously absent from the SIG is Power-One (www.power-one.com), which last year launched its proprietary Z-One bus and in December announced a design, manufacturing, and marketing agreement with C&D Technologies (cdtechno.com). According to Dave Hage, executive vice president of Power-One, "For complex systems, PMBus does not provide a configuration-controlled, standardized programming interface like the Z-One GUI. Lack of standardization in PMBus converters could make the creation and management of a uniform PMBus GUI virtually impossible."

Hage also points out that a bus architecture is overkill and adds too great an expense for some low-end designs. "For low-complexity systems, customers have requested a configurable point-of-load supply that does not require a bus and is more cost-effective." Power-One developed its "no-bus" Z1000 supplies for these applications.

—by Margery Conner

▶**Artesyn Technologies**, www.artesyn.com.

▶**System Management Interface Forum**, www.powersig.com.

▶**Power Management Bus Implementers Forum**, http://pmbus.info/specs.html.

WI-FI CHIP ATTACHES VIA PCI EXPRESS

Broadcom has released what it claims is the first 802.11 wireless-LAN chip that supports the PCI Express bus architecture. The 802.11a/g BCM4311 baseband processor integrates a MAC (media-access controller). The chip's all-CMOS design, high integration, and small footprint provide design flexibility for wireless-enabled notebook PCs, printers, and other client devices, according to Broadcom. "This is a wireless-LAN chip set with our BroadRange technology, which allows devices to hear better in noisier environments with 2- and 5-GHz-band radios," says Brian Bedrosian, Broadcom's senior product-line manager for wireless-LAN clients.

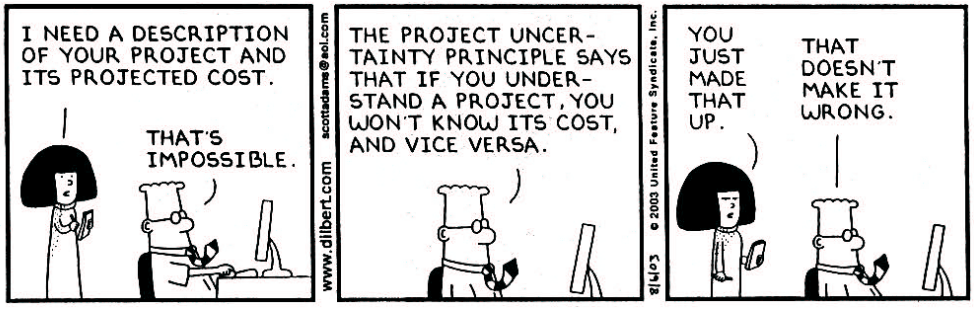
The BroadRange DSP technique allows devices to stay connected at distances as much as 50% farther from a wireless router than previous-generation technologies, according to the company. The chip's lead-free package and more efficient footprint make it a good fit for next-generation PC designs.

The device works with the company's OneDriver software, which offers various features, including SecureEasy SetUp software and 125 high-speed mode, to augment the Wi-Fi (wireless-fidelity) network. The software aims to make setup and configuration user-friendly, and the high-speed mode delivers as much as 40% greater throughput than most other 802.11g and 802.11a/g systems. Broadcom's BCM4311, available now in sample quantities, costs $10 (10,000).

–by Jeff Berman

▶**Broadcom**, www.broadcom.com.

DILBERT *By Scott Adams*



▶**The No. 1 thing consumers search for when they go to the Ask Jeeves search engine is the name of rival search engine "Google," according to Hitwide Inc, a researcher that analyzes the online activities of 10 million US consumers.**

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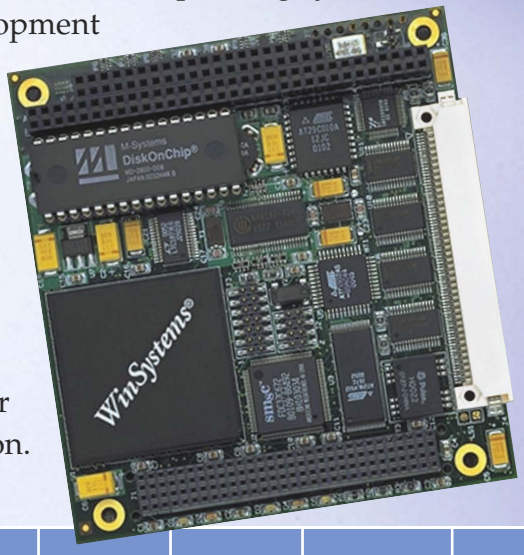

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Midpriced, 1.5-GHz-bandwidth DSOs provide an array of features

According to Boyd Shaw, product manager of Yokogawa Corp of America's Test and Measurement Division, the company's DSOs (digital storage oscilloscopes) are among the best kept secrets in the US electronics industry. Shaw says that YCA's scope sales place it fourth in the United States but that the Japan-headquartered company does far better not only in Asia, but also in Europe. Shaw believes that YCA's US DSO market share will receive a big boost from the introduction of the DL9000 series, which includes four four-channel, 1- and 1.5-GHz-bandwidth real-time-sampling scopes, whose prices start at $10,995.

In the two-channel mode, the 1-GHz units acquire 5G samples/sec on each channel. (With all channels active, the sampling rate drops to 2.5G samples/sec on each channel.) The 1.5-GHz units can sample twice as fast. At each bandwidth, you can choose between units with maximum memory depth of 2.5 or 6.25M samples/channel.

The scopes provide an impressive array of operational and connectivity features, some of which may be unfamiliar to users of US-manufactured DSOs. For example, most US suppliers have now standardized on color grading to indicate the duty ratio of pixel illumination. YCA, however, is sticking with intensity modulation, not, as you might think, because intensity modulation is less expensive or easier to implement than color grading—in a DSO, it is not—but because many users find intensity-modulated displays more intuitive. In this regard, the DL9000s' intensity-graded displays mimic analog-scope displays in a way that many users are bound to find more informative and user-friendly than color-graded displays.

The DL9000 designs go to great lengths to rapidly acquire lots of waveforms with minimal time between acquisitions and to quickly display the acquired data in the most meaningful ways. By segmenting memory when the record length is shorter than the full memory depth, the scopes can acquire waveforms with minimal time between acquisitions. One display mode uses the intensity-grading feature to create a single display that overlays the multiple acquisitions. However, all data from each acquisition remains in memory, and you can individually inspect each waveform to search for anomalies. If the accumulated length of all waveforms exceeds the memory depth, the unit discards the oldest acquisitions from the FIFO memory.

Other features include both front- and rear-panel USB ports, an optional 100Base-TX/10BaseT Ethernet interface, a trigger-comparator output for use with external equipment, a go/no-go output for use in production testing, an optional built-in strip-chart recorder, and two PCMCIA slots. (By installing an appropriate card in one of these slots, you can add an IEEE 488 interface.) The units have many built-in filtering and statistical functions. Unlike most Windows-based DSOs, these scopes run under a ROM-resident version of Windows CE. Shaw says that the results are faster start-up, greater operational stability, and more room for your data on the optional 20-Gbyte internal hard drive.

—by Dan Strassberg

▶**Yokogawa Corp of America**, 1-770-254-0400, www.yokogawa.com/us/.

DL9000 series scopes do a few things that some other DSOs can't do. For example, DL9000s can display Lissajous figures (lower half of the screen).

VOIP-ADAPTER DESIGN BOASTS $6 PRICE

Telecommunications and networking vendor Vocal Technologies has rolled out a line of VOIP (voice-over-Internet Protocol) ATA (analog-telephone-adapter) designs, including a simple ATA with a $6 BOM (bill-of-materials) cost and a full-motion IP videophone with a $30 BOM.

The designs employ DSP resources and thereby eliminate the need for an additional RISC processor, according to the company. The adapter design offers a single PSTN (public-switched-telephone-network) port and connects to a PC via USB. The design supports two telephone lines, two Ethernet lines, and a PSTN "life-line" port for automated voice-service switching in the event of a power outage or a network disconnection.

John Blume, Vocal's chief executive officer, says that these designs reduce the number of common building blocks and components necessary for developing ATAs. "Our approach to ATA is different from many others, because we eliminate the RISC processor, which, in turn, drives down the BOM for designers," Blume says. When developing its designs, Vocal looked at alternatives using both DSPs and RISC processors and found that a recent-generation DSP is suitable for running the entire application. "The idea here is to take away most of the mystery for designers and suppliers, so that they have what they need," Blume says.

–by Jeff Berman

▶**Vocal Technologies**, www.vocal.com.

▶**According to a recent report from IBM, 76% of all e-mails in February 2005 were spam, down from a summer 2004 peak of nearly 95%.**

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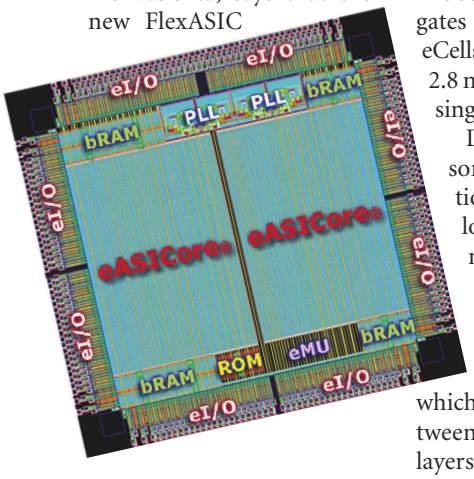
Structured ASIC offers memory-for-logic swapping

Configurable-core and structured-ASIC vendor eASIC Corp and its partner Flextronics Semiconductor have released a structured ASIC that allows users to configure the amount of logic, memory, and reprogrammable logic they need for a given design. The company's executive vice president for marketing, Ronnie Vasishta, says that the new FlexASIC fabric gives users the best of the FPGA and the ASIC worlds: the density and speed associated with ASICs without the NRE (nonrecurring-engineering) costs and the programmability of FPGAs without the power and performance shortcomings. "FlexASIC offers a 25- to 30-times density improvement over FPGAs with power density and performance akin to cell-based design," says Vasishta, claiming FlexASIC operates at approximately 400 MHz.



Implemented on 0.13-micron STMicroelectronics silicon, the FlexASIC architecture boasts as many as 3 million ASIC gates, as much as 1.5 Mbits of SRAM, and operation as fast as 400 MHz.

The FlexASIC architecture boasts a field of proprietary SRAM three-input LUT (look-up-table)-based logic cells, called eCells (embedded cells), surrounded by embedded-SRAM blocks, PLLs, an 8051 microcontroller, and ROM blocks. Configurable I/O surrounds all of these blocks. The FlexASIC architecture allows users to swap eCells for extra SRAM if a design requires. For example, the biggest device in the FlexASIC family, the FA3000, boasts 3 million ASIC gates in the form of 92,000 eCells, or 194,000 LUTs, plus 2.8 million bits of embedded single-port SRAM.

Designers can configure some eCells after fabrication to reprogrammable-logic blocks. The companies program a device's eCells, RAM, and embedded RAM during fabrication using "e-beam" technology, which customizes the vias between the sixth and seventh layers of the eight-layer process. The routing customization differs from programming the logic and programmable-logic blocks. The companies use a bit stream for this programming and can reload the blocks for debugging after fabrication.

The companies also built a clock tree into the fabric, which means that users need not build it but also that they can't adjust it. The companies offer users two design flows to configure and program the devices. Using the first flow, designers feed a Verilog or VHDL netlist into Synopsys' (www.synopsys.com) Design Compiler, which creates a gate-level netlist. Users then perform chip-resource allocation, assigning memory, clocks, and I/O on the design. Then, using a proprietary eTools suite, users perform mapping, placement, and, with technology from OEM Golden Gate Technology (www.ggtcorp.com), global routing. Users then perform final routing, finishing, and BIST (built-in self-test) with eASIC tools. They can use any vendor's tool to perform ATPG (automatic-test-pattern-generation) testing. With the second flow, users feed a Verilog or VHDL netlist into an eASIC\Flextronics-only version of Magma's (www.magma-da.com) Blast SA, which incorporates the Aplus physical-synthesis tool. The tool performs synthesis and placement and then feeds into eASIC's router, finishing tools, and BIST. As with the other flow, users can perform ATPG with any vendor's tool.

The companies currently fabricate the FlexASIC devices on STMicroelectronics' (www.st.com) 130-nm process. The companies claim that customers incur no NRE charges; eASIC and Flextronics accommodate low-volume orders because they can implement a number of customers' designs, even if targeting a different part number of the eASIC family, on a single wafer. Vasishta says that companies have ironed out the lithography and design-for-manufacturing issues. A debugging technology is available, but customers can receive sample silicon as early as two weeks after tape-out so they can test their designs in their systems in real time. Package support for the family ranges from 100-pin TQFPs to 896-pin FBGA packages; eASIC is currently receiving tape-outs from beta customers and expects prototyping silicon by May and production silicon by July.

—by Michael Santarini

▶**eASIC**, www.easic.com.

▶**Flextronics**, www.flextronics.com.

Even jacks are getting smarter

Though not the first jacks in audio's history with an auxiliary function, a new series from FCI USA brings the concept to the 38.5-mm-high BTX (Balanced Technology Extended) form factor, as well as to the 38.5-mm-tall jacks for the ATX (Advanced Technology Extended) form factor. The company's Smart Audio Jack series of triple-stack connectors features an isolated switch so that associated circuitry can detect connector presence and also sense when a microphone, an audio input, or a speaker is plugged into the port. (Some designs use an electronic-circuit technique to make the same determination, but that approach can become complex because the jack must sense a completed—but highly variable and uncontrolled—signal path.)

The color-coded jacks, targeting 192-kbps, high-definition audio designs, have initial 50-mΩ contact resistance and are rated for 1A current and 1000 insertion cycles. Price is 32 cents to 68 cents (1000), depending on configuration.—by Bill Schweber

▶**FCI USA**, www.fciconnect.com.

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FPGA development kit targets designs that "race"

Mercury Computer Systems has rolled out a development kit supporting the company's FPGA computing systems that employ its high-speed Race++ switch fabric. The FDK (FPGA Compute Node Developer's Kit) 2.0 platform, which includes software, IP (intellectual property), and design consultation, offers the interconnect, communications, command and control, memory, and I/O functions for flexibility and quick deployment, according to the company.

The kit supports the company's IP cores for the ROC (Race-on-chip) high-bandwidth interconnect, a patent-pending technology that extends the fabric inside the FPGA to access other IP cores, such as high-speed DRAM, SRAM, sensor-I/O, and system-level fabric interfaces, according to the company. The kit supports the PCI-based VantageRT FCN (FPGA-based compute node) and VME-based MCJ6 FCN systems. Both of those products feature multimillion-gate Xilinx (www.xilinx.com) FPGAs connected to Race++, which is Mercury's implementation of the industry-standard Raceway Interlink high-performance interconnect fabric.

Rich Jaenicke, Mercury's director of product management, says that FDK 2.0 helps users load bit streams into their FPGA and IP, providing an FPGA interface to components such as memories, switch fabric, and I/O. "Users have data streaming from a sensor into an I/O interface and are computing and storing data in memory and sending results over the switch fabric," Jaenicke says. "We are providing infrastructure interfaces, which are helpful for our customers, because this approach allows them to focus on algorithms and not have to spend time on infrastructure." Engineers will also find the kit beneficial because it includes a dual DMA master/slave switch-fabric endpoint. "Switch fabrics are all the rage now, and this IP says that we have the switch fabric and all the protocol layers directly on the chip," Jaenicke says. FDK 2.0 is available now and costs $23,000 for the first development seat, which includes 20 hours of development support.

—by Jeff Berman

▶**Mercury Computer Systems**, www.mc.com.

Single-chip FM tuner enables embedded broadcast receiver

What would EH Armstrong say? The FM (superheterodyne) pioneer never envisioned an all-CMOS, single-IC FM tuner, such as the Si470x series from Silicon Laboratories. This highly integrated, 4×4-mm digital component needs just a bypass capacitor and takes less than 20 mm^2 of board space overall, far less than the typical approach, which requires a 6×6- mm IC, more than 30 support components, and 150 mm^2 of space.

The single-chip tuner, the vendor asserts, is the industry's first all-CMOS device. It simplifies embedding a conventional broadcast FM receiver, spanning 76 to 108 MHz, into a cell phone or an MP3 player, for example, and thus it is "easy and cost-effective to add FM radio as a standard feature to virtually any application," according to Ed Healy, vice president at Silicon Labs. And, even if you think broadcast radio is dead, many consumers do not; it is increasingly a feature on portable wireless devices.

The Si4700 version needs no alignment. It includes the required filtering, AGC (automatic gain control), a frequency synthesizer with a VCO (voltage-controlled oscillator), a low-dropout amplifier for direct battery connection, and audio-processing functions. The Si4701 adds an integrated preprocessor for the European RDS (Radio Data System) and the US RBDS (Radio Broadcast Data System) formats at a 57-kHz offset, which adds station ID and song name along with the music and allows alternate-channel (frequency) information, which European radio provides, in which a single broadcaster uses multiple frequencies.

The Si4700 sells for $3 (10,000), and the Si4701 sells for $3.50. The companion evaluation board costs $150.

—by Bill Schweber

▶**Silicon Laboratories Inc**, www.silabs.com.

The all-digital, CMOS Si470x FM tuner does it all and in a 4×4-mm package, allowing designers to easily incorporate broadcast tuning into wireless handheld products.

▶**Checks accounted for 45% of all payments that were not made with cash in 2003, down from 57% in 2000, and 32% of US households used the Internet to pay bills in some fashion in 2004, according to TowerGroup.**

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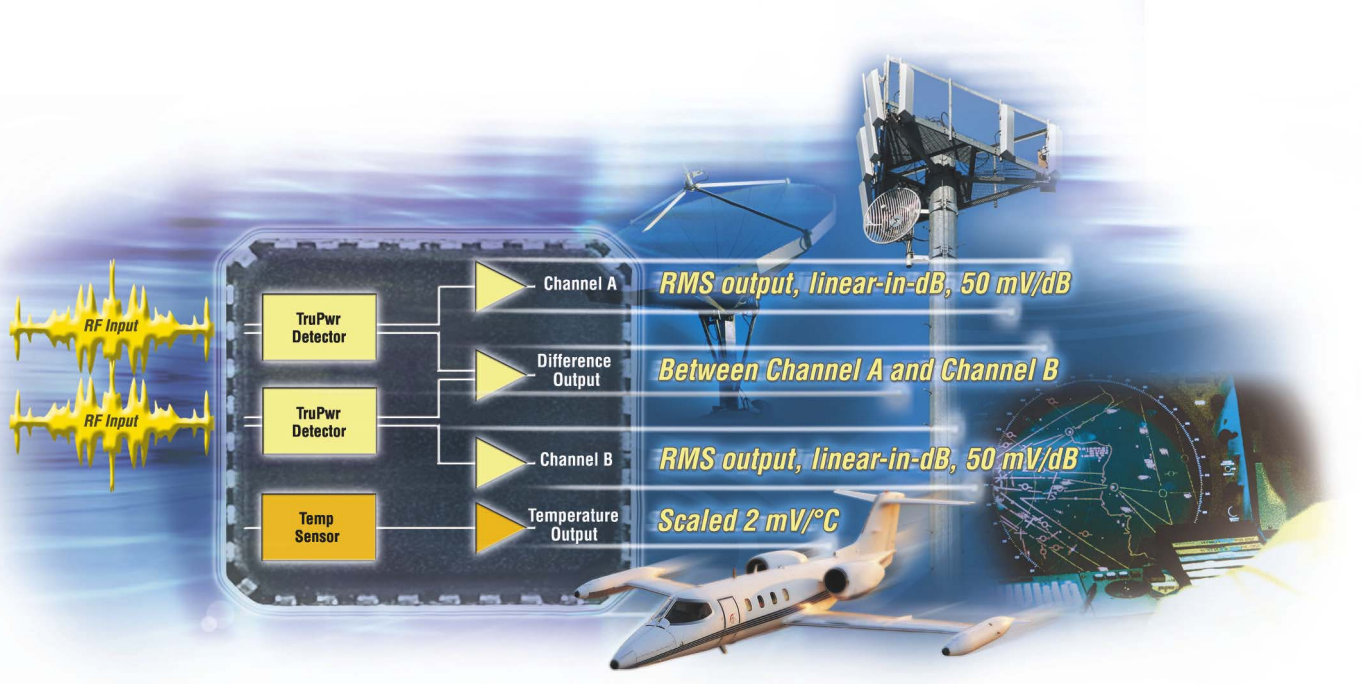

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Crosstalk in differential vias with grounds

In 2002, the XFP (10-Gbit small-form-factor pluggable-module) committee, working on standards for 10-Gbps interconnections, published some terrific guidelines for high-speed differential vias (**Reference 1**). The guidelines propose surrounding your differential pair with an oval clearance and pinning the reference planes together at either end of the clearance hole with ground vias (**Figure 1**).

The guidelines assume that no long dangling via stubs connect to your signal path, meaning that either (a) your signal goes all the way from the top layer to the bottom, or (b) in a less-than-full-length transition, you have cut off the dangling ends of the via beyond the point at which signal current actually flows.

In boards as thick as 100 mils and with rise times on the order of 100 psec, the recommended structure produces a good, 100Ω transition between layers.

If you want to use this design in a dense architecture, you need to know about the crosstalk between these structures. To make the math easy, I will assume your layout provides a uniform grid of possible via locations, with a grid spacing of 0.8 mm and hole diameters of 0.3 mm. Index the grid by rows and columns.

Place one installment of the layout from **Figure 1** with the topmost via at position Row 0, Column 0. The crosstalk voltages (millivolts) into this spot from other possible via locations appear in **Table 1**. For example, placing an aggressor pair one position to the right (one column over), the crosstalk from **Table 1** in position Row 0, Column 1, reads 42 mV. I did these quasi-static calculations using MathCad.

Because the layout in **Figure 1** is four positions long, if you stay in the same column, the closest you can place the next structure (shifting straight down) is four units. The shaded areas in the **table** designate impossible positions.

This **table** assumes a 2V p-p differential signal (that is, 1V p-p on each wire), driving 100Ω differential traces with 100-psec rise and fall times. The important aspect of this specification is the total change in current per unit time (*dI/dt*). Crosstalk in millivolts scales in proportion to d*I*/d*t*. If you have a lower voltage, a slower rise time, or a larger trace impedance, then scale down the numbers in **Table 1** according to the extent of that difference in your architecture. As the **table** shows, crosstalk quickly plummets to small values as you separate aggressor from victim. Enforcing white space between signals is the surest way to guarantee low crosstalk.

What happens if you omit the ground vias? In that case, signals pass through the via in much the same way, but the crosstalk floats generally higher. More important, crosstalk falls off less rapidly with distance (**Table 2**). Ground vias help contain the electromagnetic fields emanating from each differential structure, arresting the spread of crosstalk.□

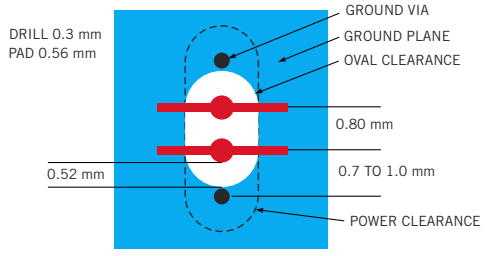

Figure 1 These proposed pc-board-layout dimensions for 10-Gbps standards help with proper performance.

TABLE 1—CROSSTALK IN MILLIVOLTS WITH GROUND VIAS

Row/Column	0	1	2	3	4	5
0	0	42	5	1	0	0
1	0	23	1	0	0	0
2	0	3	2	0	0	0
3	0	3	0	0	0	0
4	1	0	0	0	0	0
5	0	0	0	0	0	0

TABLE 2—CROSSTALK IN MILLIVOLTS WITH GROUND VIAS REMOVED

Row/Column	0	1	2	3	4	5
0	0	85	27	13	7	5
1	0	14	15	10	6	4
2	35	14	1	4	4	3
3	14	10	3	0	1	2
4	8	6	4	1	0	1
5	5	4	3	2	1	0

Reference

1. 10-Gigabit small-form-factor pluggable module, Revision 2.0, XFP multisource agreement.

Howard Johnson, PhD, author of High-Speed Digital Design *and* High-Speed Signal Propagation, *frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. howie03@sigcon.com.*

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Perception problem dogs engineering

Luring college-bound students into engineering has never been more difficult. From an attractiveness standpoint, engineering enjoyed brief life during Internet's early years, but has since returned to the more conservative realm that encourages only math and science geeks. Since 1990, the number of bachelor's degrees in engineering has dropped 8%. More disturbing is a 20% decline in math degrees (**Link 1**).The reason for these declines is twofold, according to Geoffrey Orsak, School of Engineering dean at SMU (Southern Methodist University): One is that high-school students often shun science and math; most avoid taking them in college if they can. The other problem is image, and we can do something to improve it, contends Orsak, who is the antithesis of the engineering stereotype that, fairly or unfairly, has long tarnished the profession's image.

"Most believe it's one of the toughest majors, and so we are competing over a very small group of kids. But clearly engineering has an image problem even more than the perception that it's a challenging discipline," he says. That salaries for new engineers are among the highest compared with other professions doesn't seem to matter. "People see it as a bridge career from lower working class to a middle-class career. Once you reach that level, you want to go beyond it into law, medicine, and business leadership," he says.

That idea surprises me. I always admired people with a strong aptitude for math and science, probably because the two were not my strong suits. My civil-engineer uncle built interstates for 39 years, and I admire him. As a 19-year-old, his formidable math skills and intestinal fortitude landed him in the navigator's seat of a B-24 during World War II and in an Rensselaer Polytechnic Institute classroom after that on the GI Bill. My 17-year-old son just aced the SAT II test in math. What does he want to be? A lawyer.

The decline in US engineers has become more noticeable because developing economies in countries such as China are cranking out new ones at four to six times the rate in the United States. And strong growth in retirements as the engineering workforce ages will compound the problem. More than half of the engineers in the United States are older than 40, says the NSB report.

WE CAN'T LOWER THE ACADEMIC BAR, SO WE HAVE TO INSTEAD SPRUCE UP ENGINEERING'S IMAGE.

What can the United States do about this problem? Clearly, we can't lower the academic bar, so we have to instead spruce up engineering's image. "We have to celebrate our people. As long as we continue to view engineering as about widgets and not about people, we will have a perception problem," says Orsak. Engineering needs highly visible heroes, just as the business world has Michael Dell and Bill Gates. Such heroes motivate students to take a similar path. But engineering has plenty of Dells and Gates. The problem is that they generally don't seek recognition, except, perhaps, from peers. There are plenty of successful engineers, but they either labored in obscurity or took another path. Former General Electric Chief Executive Officer Jack Welch is a chemical engineer. Jimmy Carter is a nuclear engineer. Yasir Arafat was a civil engineer (**Link 2**). "If a doctor develops a new surgical technique, we celebrate it. We don't do that in engineering. I could name 10 famous doctors, but I could not name 10 famous engineers," says Orsak. That's why SMU has partnered with Texas Instruments to develop the Infinity Program, which attempts to dispel the myths and stereotypes that plague engineering in high-school classrooms (**Link 3**). The program trains high-school math and science teachers to make engineering fun, cool, interesting, and accessible to broader range of prospects.

That the numbers of new engineers hasn't changed for decades indicates the magnitude of the problem. And what we do now to convince more high-school students to choose engineering won't pay off in national competitiveness for a decade. Currently, approximately 65,000 engineers a year graduate from US schools, says Orsak. "It's never been over 100,000 and never below 50,000 for the past 30 years. But many more kids go to college today, and we thought a rising tide would lift all boats."□

Do you have an engineering hero? Write me at john.dodge@reedbusiness.com.

Links

1. "Science and Engineering Indicators 2004," National Science Board, www.nsf.gov/sbe/srs/seind04/c0/c0s1.htm.

2. *The Encyclopedia Britannica,* www.britannica.com/nobel/micro/30_1.html.

3. www.infinity-project.org/join/join_video.html.

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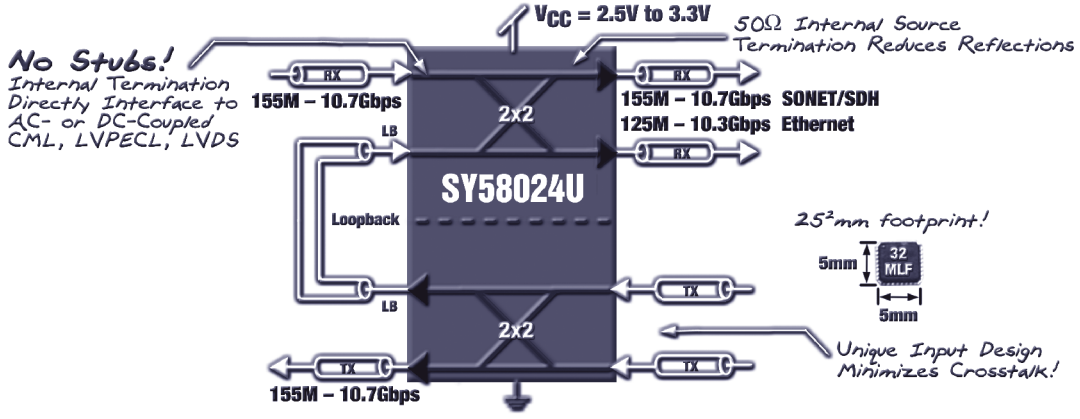

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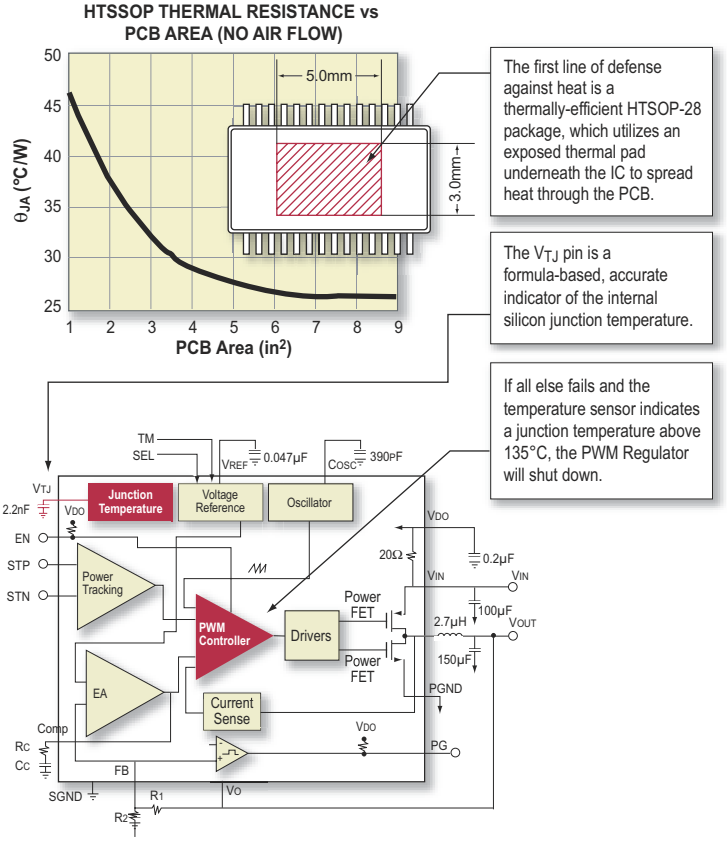

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 By David Marsh, Contributing Technical Editor

THE GROWTH OF ELECTRONIC SUBSYSTEMS IN VEHICLES DEMANDS NETWORKS FROM THE MISSION-CRITICAL TO THE MUNDANE. THE LOCAL-INTERCONNECT-NETWORK PROTOCOL TACKLES THE TASK.

LIN simplifies and standardizes IN-VEHICLE NETWORKS

With predictions suggesting a global annual-compound-growth rate of some 8.3% over the next five years, the automotive sector continues to be our industry's fastest growing market. It's sobering to consider that, barely 20 years ago, the sole electronics content within most vehicles was a radio. Then came the electronic ignitions, engine-management units, and antilock-braking systems that are standard in today's entry-level cars. Now, of course, vehicles include previously unheard-of luxuries, and top-of-the range vehicles adopt sophisticated electronics, such as intelligent cruise controls that automatically maintain a safe distance from the vehicle ahead. Estimates suggest that the electronics content of an average car now accounts for no less than 22% of its manufacturing cost, creating markets for the embedded controllers, power devices, and communications technologies that link its ECUs (electronic-control units).

Recognizing the need for a robust in-vehicle network to manage distributed intelligence and reduce wiring-harness dimensions, Bosch in 1986 designed a CAN (controller-area network). Today, CANs dominate in-vehicle networking and have also made the transition to multiple industrial uses. In the meantime, other networking systems have appeared to tackle emerging automotive applications. These technologies include D2B (domestic-digital-databus), FlexRay, and MOST (media-oriented system transport), all of which employ fiber media for speed and EMC resistance. TT-CAN (time-triggered extensions to CAN) improve the protocol's determinism, as well as the TTP (time-triggered-protocol) series that competes with FlexRay for safety-critical use (**Reference 1**). Because these systems serve high-end applications and are relatively expensive, designers require a low-cost alternative to serve mundane tasks, such as to control body functions from seats to sunroofs. As a result, car makers increasingly embrace LINs (local-interconnect networks), which position themselves at the lowest level in the automotive-networking hierarchy (**Figure 1**).

The first LIN specification appeared in 1999. Among the founding members of the LIN Consortium, its design authority, are car makers BMW, DaimlerChrysler, Volkswagen Audi Group, and Volvo Cars, together with hardware and networking expertise from Freescale Semiconductor and Volcano Automotive Group. Design influences include the Vlite bus that several car makers use, as well as lessons accruing from many years of CAN evolution and development. Several amendments culminated in LIN Version 1.3 in November 2002, which many observers regard as the first stable release. Further work resulted in a major revision that appears as the current Version 2.0 of September 2003, which the LIN Consortium recommends for all new development.

Meanwhile, in North America, the Society of Automotive Engineers issued its J2602 recommended practice, "LIN Network for Vehicle Applications," with key car-maker representation coming from Ford and General Motors. The main differences between LIN 2.0 and J2602 include limiting the transmission rate to 10.4 kbps and modifying some protocol details, such as error handling. Some observers feel that J2602's objectives include limiting feature creep, thus making it easier to meet LIN's overriding low-cost target using, for example, state-machine logic rather than microcontroller-based intelligence.

The LIN Consortium's objectives for its new system don't stop with low cost, although, because LIN is markedly cheaper than CAN or the J1850 domestic-US standard, cost is the prime driver. In fact, with original predictions for LIN lying at around $1/node, it is currently proving hard to meet this cost target. But, in its primary role as a sub-bus, LIN's design ensures that it functions as a logical and scalable extension of CAN and J1850. It provides acceptable reliability for nonsafety-critical tasks, with less-than-100-msec response times and predictable worst-case timing characteristics. Learning from previous bus evolutions, the developers were also careful to consider tool-chain-support issues. Such considerations have become crucially important as the car makers forge seamless co-development links with their system suppliers.

Naturally, the specification must ensure hardware and software interoperability among multiple vendors, as well as minimizing peripheral but critical issues, such as EMC. From the outset, LIN's specifications accordingly subdivide into three main parts that describe the transmission medium and its communication protocols, a configuration language, and APIs (application-programming interfaces) (**Figure 2**). Representing the lowest two levels of the ISO/IEC 7498-1:1994 open-systems-interconnect model, the protocol specification tackles the physical-layer and data-link-layer mechanisms. At the highest level, an API abstracts the user's code from lower level network mechanics; in between, a signal interaction and diagnostic layer decouples the application from the network. To furnish a standard interface between LIN nodes from multiple suppliers, the LIN configuration-language description defines the format of the files that configure the network. These configuration files also provide hooks into development tools. In a further and major forward step, 2.0 introduces the LIN-node-capability language, easing integration via a plug-and-play concept (see **sidebar** "LIN 2.0 goes plug and play" on the Web version of this article at www.edn.com).

AT A GLANCE

- ▷ LIN (local-interconnect network) challenges CAN (controller-area network) for lowest cost in noncritical applications.
- ▷ Version 2.0 introduces new plug-and-play capability but costs memory.
- ▷ Vendors offer a dazzling palette of hardware support.
- ▷ Future growth prospects include consumer goods and industrial use.

ONE-WIRE MASTER/SLAVE ARCHITECTURE

To minimize cost and wiring weight, LIN uses a single-conductor, wire-OR bus that takes advantage of a car's body shell to serve as a common ground. Each LIN subnet comprises one master and at least one slave node to a maximum of 16 devices per bus. Nodes can participate on more than one LIN bus, and masters may also operate as bridges into other network environments, typically CANs. Maximum transmission speed and reach are 20 kbps and 40m, respectively, using UART/SCI communications. This technology makes LIN implementations pos-

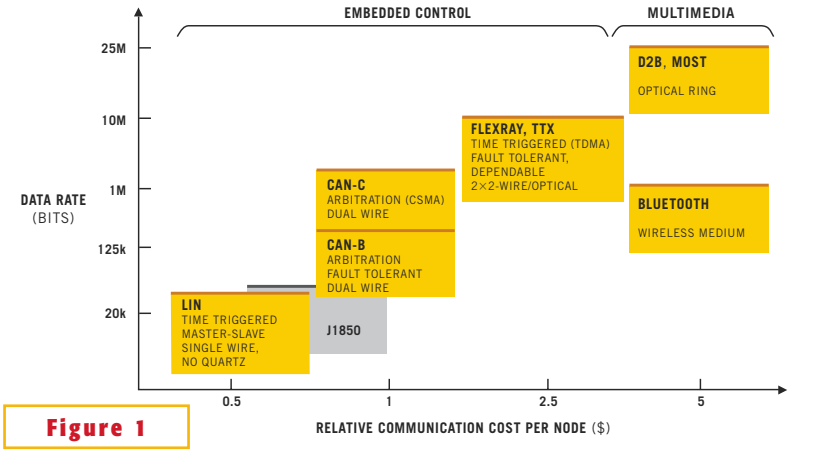
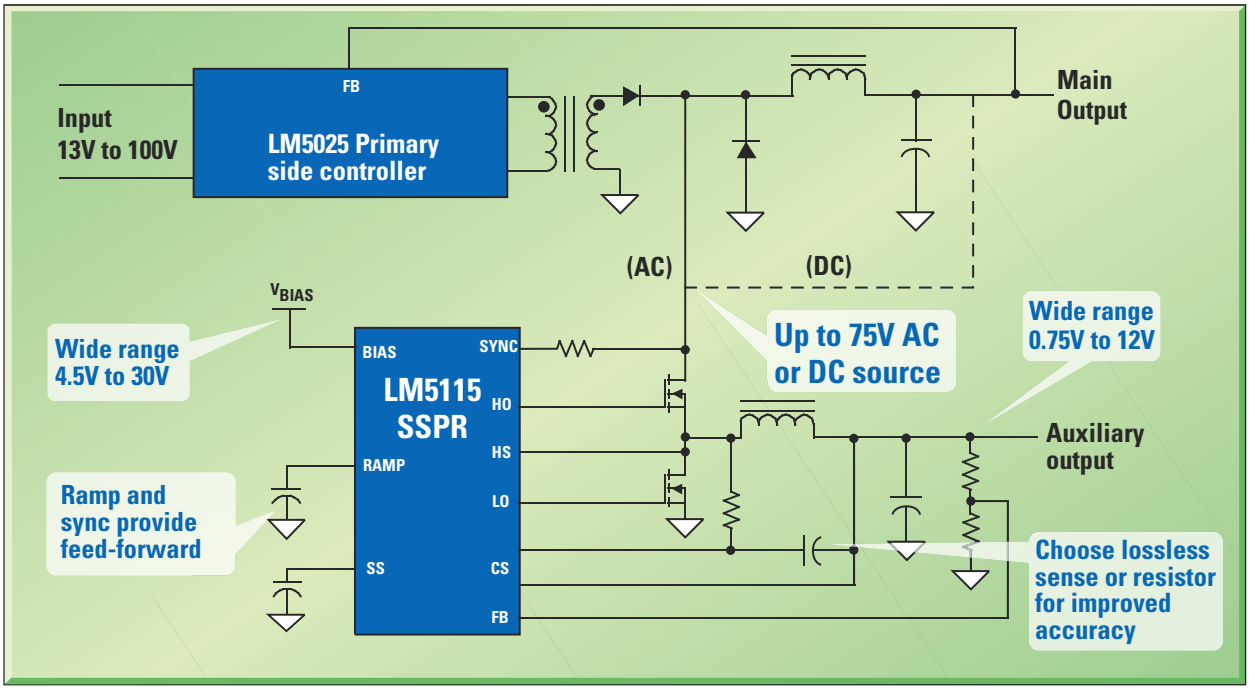


Figure 1

LIN tackles the lowest level of the in-vehicle-networking hierarchy.

Secondary-side post regulator (SSPR) doubles as high-voltage DC-DC controller

Feature-rich LM5115 controller simplifies design of multiple output DC-DC converters



LM5115 Features

- Provides multiple outputs from main DC-DC or AC-DC converter
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- Leading-edge modulation for SSPR from current-mode primary controller
- Up to 1 MHz switching frequency reduces component footprint and profile
- Integrated gate drivers with 2.5A peak output current
- Available in TSSOP-16 and tiny LLP-16 packaging

Ideal for use as a secondary-side post regulator in the design of multiple output AC-DC or DC-DC power supplies or as a DC-DC controller for use in point-of-load (POL) regulators

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Shown actual size

LLP-16
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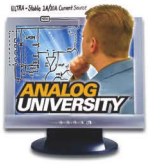

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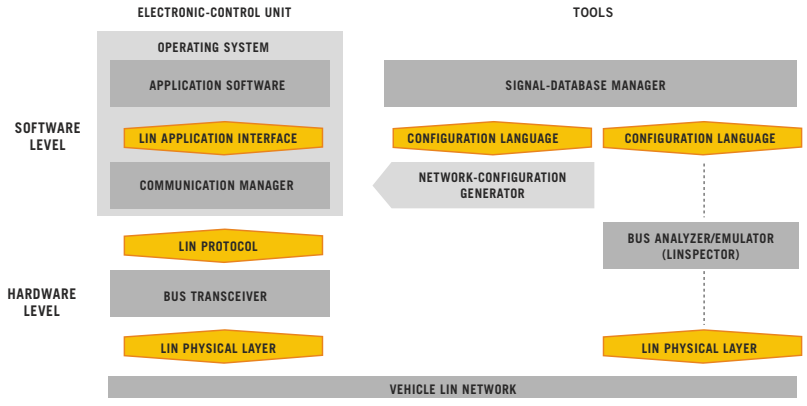

Figure 2 **LIN defines the physical-layer, protocol-handler, and application-programming interfaces with support from a configuration language.**

sible with drivers ranging from simple state-machine logic to "bit-bashing" an I/O pin in software to using serial peripherals. Such low speeds also constrain interference generation and ease timing issues, assisted by a master-driven self-synchronization facility that allows slave nodes to dispense with crystal or resonator timers.

Physical-layer exchanges employ an enhancement to the ISO-9141 standard that dominates European and Japanese vehicle-diagnostic systems. LIN-compatible line drivers limit slew rate to around 2V/μsec to avoid creating interference due to fast edges. Such a line driver asserts the "dominant" logic-zero state by driving the bus line to within 20% of system ground; a "recessive" logic one requires driving the line to within 20% of battery voltage. To allow for effects such as ground shift, receivers allow more tolerance, acknowledging levels within 40% of the respective rails (**Figure 3**). The master terminates the bus with a 1-kΩ resistor to battery voltage, and each slave defaults its I/O line high with a 30-kΩ pullup resistor. A diode in series with the termination resistor prevents devices on the bus from backfeeding into the battery-voltage rail if the supply fails. Masters and slaves also each present around 220 pF to the line up to a maximum of 10 nF per bus, which results in a system time constant of 1 to 5 μsec. In a region in which AM radios still proliferate, SAE-J2602's 10.4-kbps limitation further eases compatibility issues for the North American market.

Unlike CAN, LIN's master/slave architecture avoids data-traffic collisions and the need for arbitration logic by having the master supervise message transmissions, thus ensuring that only one message transmits at any time. A frame consisting of the master's header, a pause, and a slave's response encapsulates each message exchange (**Figure 4a**). Start and stop bits surround each byte, resulting in a 10-bit transmission per byte. There are several frame types, starting with diagnostic frames that carry diagnostic or initialization information. By contrast, "unconditional frames" always carry signals of as many as eight bytes. These are the frame types typify applications. "Sporadic" frames also always carry signals, but slaves respond only if new data is available, otherwise leaving the data field blank—an attempt to add some dynamic behavior into the system's schedule without compromising its determinism. Polling infrequently responding nodes generates bus traffic. To improve system responsiveness by reducing the bus traffic, the protocol includes an event-triggered frame. This frame accommodates as many as seven data bytes, because the first field carries an identifier that associates the frame with its task. Again, slaves respond only if they have new data. The protocol also provides for user-defined frames and reserves another type for future use.

To initiate a data transfer following an interframe space or bus-idle condition, the master transmits a header comprising a synchronization-break period, a single-byte-synchronization field, and an identifier byte. The identifier byte carries six bits of information and two parity bits, allowing 64 message identifiers (**Figure 4b**). In normal operation, there is no addressing as such; rather like CAN, the identifier byte uniquely defines the purpose of the frame. Identifier decimal values of zero to 59 carry signals; 60 and 61 are master-request and slave-response diagnostic frames, respectively; user-defined frames have a header value of 62; and 63 is reserved. Each slave waits for the synchronization break and locks onto the synchronization byte before scanning the bus message. One or more slaves then receives data, or a single slave transmits response data. The data field accommodates eight bytes; the data field's association with its identifier byte predefines the field's length. A single-byte check field terminates the transmission, providing an error-detection facility. The master is responsible for all error handling, which is in turn the application programmer's responsibility; LIN 2.0 has no defined error-handling mechanism.

Because it's imperative to preserve battery power when the vehicle is inoperative, slaves automatically enter sleep mode if the bus is idle for more than four seconds. The master can also force slaves into sleep mode by sending the diagnostic master-request frame with the first data byte set to zero. The master subsequently monitors the bus when it is idle, looking for wake-up signals from slaves that require service. Any bus node can request wake-up by asserting the dominant state for 250 μsec to 5 msec, which makes 5 msec the dominant state's longest valid

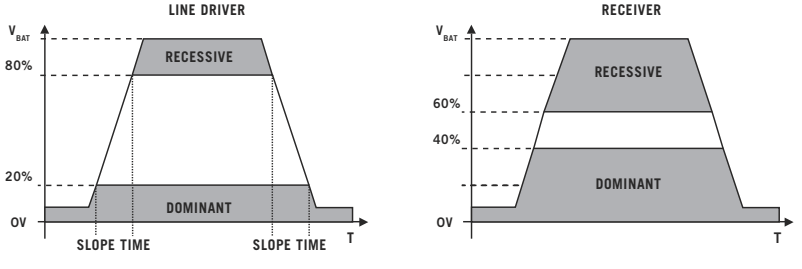

Figure 3 **Receivers tolerate levels of as much as 40% of the supply rails to account for effects such as ground shifts.**

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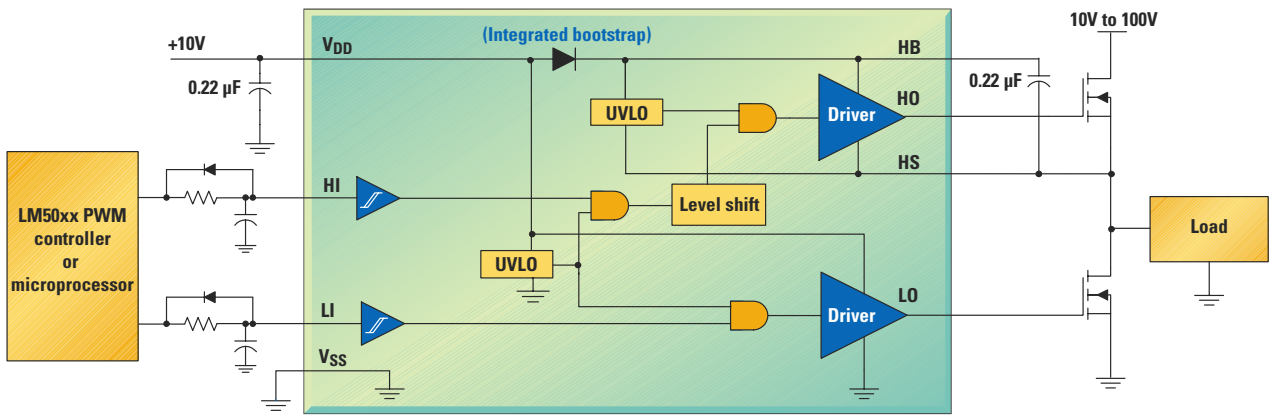
LM510x Typical application circuit



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Peak Gate Current	Product ID	Input Threshold	Packaging	Comments
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NEW! 1.8A	**LM5105**	TTL	LLP-10	Programmable dead-time, negative V_{LOAD}
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run. Most transceivers incorporate a watchdog timer that disconnects nodes exceeding this maximum, because such behavior indicates an error condition that would otherwise monopolize the bus. Slaves must wake up and be ready to transmit data within 100 msec of the end of the wake-up signal. Crucially, because the message length, interframe-spacing parameters, and device-wake-up times are known, it's easy to calculate worst-case response times for any system. Masters typically use a static, round-robin scheduler, although adaptive schedulers provide greater flexibility to permit decision-based systems that similarly have guaranteed determinism.

An exception to the zero-collision rule occurs when the master polls for an event-triggered frame and more than one slave responds within the same time slot. This situation might arise, for example, when the master polls all the doors within a central-locking application using an event-triggered frame. The response would normally be blank, but if more than one door button is active at this instant, more than one slave responds. The master resolves the collision by requesting all of the unconditional frames of similar association and checks their event flags before again requesting the event-triggered frame. This sequence avoids the possibility of a slave's withdrawing from a collision without corrupting the data, which the master would not detect, and thus lose the slave's response. Because application software implements these sequences, the programmer must ensure that the bus has enough time to complete its operations without compromising the system's schedule. At the scheduler level, it's not permissible to include unconditional frames that are associated with either a sporadic or an event-triggered frame within the same schedule table as the sporadic or the event-triggered frame.

SIMPLICITY BELIES CHALLENGES

Although LIN is conceptually simple, device vendors still face significant challenges. The first difficulty is to fabricate bus transceivers that withstand automotive conditions, notably severe EMC-test compliance. Although LIN constrains interference generation through baud- and slew-rate limiting, it's important that the system withstands severe levels of radiated and conducted emissions. Against a background of emissions and interference issues, car makers have developed a range of in-house tests for evaluating in-vehicle networks. These essentially consist of injecting RF interference into the bus and varying the signal's frequency, amplitude, and modulation depth until the system fails. Many common elements of these proprietary tests appear in the LIN-conformance test suite, which agencies such as the Communication and Systems Group at Fachhochschule University of Applied Sciences specialize in applying on behalf of its clients.

Scott Monroe, system architect at Texas Instruments' mixed-signal power and control group, explains that bulk-current-injection tests are popular in the United States, whereas European car makers favor DPI (direct-power-injection): "With DPI, you increase the RF-power levels into a bus of, say, three or four transceivers, via an RC coupler until the system breaks. With bulk current injection, the bus runs through a coupling coil, and you again vary the interference levels, looking for the point where message transmissions fail." Monroe notes that the LIN specifications don't mention protection against reverse-battery faults and negative-going transients, such as those that inductive loads create. These tests form part of the CISPR (International Special Committee on Radio Interface)-25 and ISO (International Organization for Standardization)-7637 transient-immunity standards for automotive ICs. With a ±40V bus fault and as much as 17-kV ESD protection, TI's TPIC1021 withstands these rigors and improves system reliability with features such as dominant-state time-out. Its I/O pins use a 5V-tolerant 3.3V structure for maximum logic compatibility. With thermal and bus-terminal protection from shorts to either supply rail, the chip doesn't disturb other bus communications in its inactive state. It responds to wake-up requests from the bus, from an enable pin that connects to the host microcontroller, or to a battery-voltage level-switch input. In sleep mode, quiescent current consumption falls from a maximum of around 2.5 mA to about 20 μA. The chip can also control an external voltage regulator, making it possible to power down a microcontroller or other LIN-protocol logic.

Other vendors that offer LIN transceivers include AMI Semiconductor, Atmel, Freescale, Infineon, Melexis, Microchip, On Semiconductor, Philips, STMicroelectronics, Yamar, and ZMD. Like the TI part, many of these devices offer similar pinout and functions to Freescale's MC33399 and Philips' TJA-1020 market-leading transceivers. Philips has a useful application note that illuminates LIN-transceiver issues (**Reference 2**). There are, however, detail differences between the electrical specifications in various competitive products, such as in the fault-voltage tolerance that vendors quote. For example, Atmel's ATA6661 withstands bus voltages of as much as 60V for use in 42V PowerNet environments. There are also some subtle differences between apparently similar pinouts. For example, although most transceivers run directly from the vehicle's battery voltage, On Semiconductor's NCV7380/7382 requires a 5V supply on Pin 3, which is typically a battery-voltage-compatible wake-up-signal pin. The NCV7380 variant also dispenses with sleep-mode logic to minimize cost.

Gilles Guillaume of On Semiconductor's European marketing operation notes that the company offers designers extra flexibility, such as a voltage-regulator option to derive auxiliary power. In-

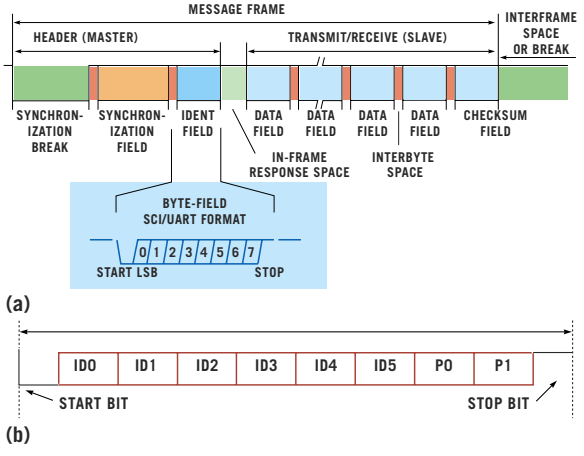

Figure 4 Each message exchange comprises a master-initiated header followed by a slave's reception or transmission (a). The master sends an identifier byte that uniquely defines the frame's purpose within a system (b).

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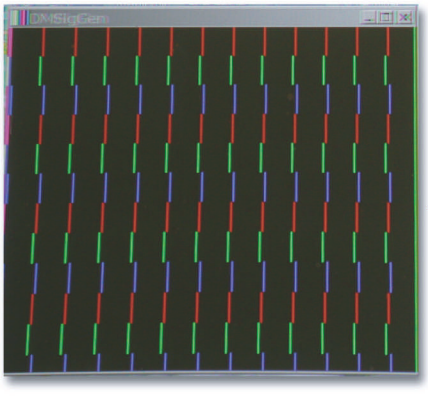
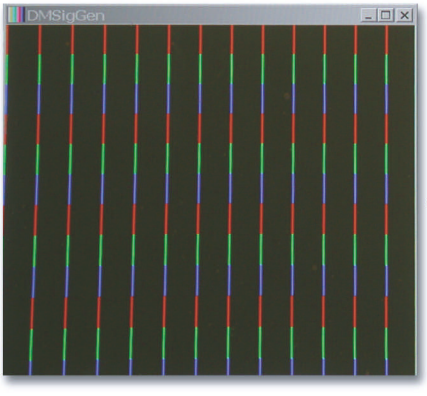
Video Performance Over CAT-5 Cable Driving You Crazy?

Intersil's EL9115, a triple analog delay line, compensates skew introduced by CAT-5 cable, enabling high-quality video through 1,000 feet of cheap twisted pair cable.

The EL9115 allows three channels to be independently delayed in 2ns steps, up to 62ns. This allows de-skewing of signals, such as RGB video that is transmitted over CAT-5 cabling. Now signals can be exactly aligned at the receiver for a razor-sharp image.



Video transmitted over 1000 feet of CAT-5. Note the lack of alignment on the RGB test pattern.



EL9115 is programmed to align the RGB vertical test bars. De-skewing required 44ns delay on green and 18ns on red. The test bars now line up vertically.

Features

- 62ns total delay
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tegrating a low-dropout-voltage regulator, the company's NCV7361A employs a modified eight-pin format to provide a 5V, 50-mA output. Melexis offers a similar part with its TH8061. Other examples of transceivers with integral voltage regulators include Microchip's MCP201, which trades the typical Pin 3 wake-up function to furnish a 5V, 50-µA output. An external pass transistor can boost this capability for more demanding loads. An enhanced version, the MCP202, with higher ESD resistance and lower standby current will become available for sampling this summer. Texas Instruments also plans a transceiver variant with voltage-regulator-output capability.

MICROCONTROLLERS PLAY STATE MACHINES

The low cost and competitive nature of the LIN market complicate system integrators' choice of architecture. This choice even may differ within the same system due to the requirements of masters and slaves. Traditionally, pc-board designers gain maximum flexibility by using separate transceivers and microcontrollers. Because designers build these devices around a familiar product family and development-tool chain, this route is often a favorite, especially for masters. It may also provide an easy bridge into a CAN environment. Alternatively, microcontrollers with onboard transceivers and application-specific peripherals provide tightest integration, shrinking size and potentially offering the lowest cost for high-volume applications. Ross Mitchell, 8/16-bit-system software-application manager at Freescale, notes that size is often crucial, because trying to integrate, say, a mirror controller within plastic molding can prove challenging: "It's typically desirable to have the control module as close as possible to its load, because this strategy minimizes wiring and can improve EMC performance."

But for lowest cost, state machines challenge microcontrollers and expensive on-chip memories. Such memories are necessary for supporting in-system configuration, which is one reason that some users want to stay with hardware that is compatible with LIN 1.3. Microchip's Johann Stelzer, European marketing manager for automotive products, believes that US customers in particular will adopt a subset of 2.0: "From a cost viewpoint, diagnostics and in-system configuration are a negative developments that threatens the $1/node target," he says. More than one competitor acknowledges that today's low cost of CAN may erode the advantages of a complex LIN implementation. According to TI's Monroe, the optimal balance is crucially application-dependent. His company is supplying system makers with fully integrated products based on both state-machine and intelligent logic, although these devices are not yet available as catalog items. Many of these custom devices are three-pin slaves that fulfill roles as diverse as oil-quality and temperature sensors for engine-control systems to seat-weight sensors for occupant detection.

Monroe says, "From the lowest cost viewpoint, constraining feature creep and keeping it simple are obviously the ways to go." But in common with his peers, Monroe recognizes that there is a tendency among some designers to desire ever more features. As a result, a staggering array of controller options are

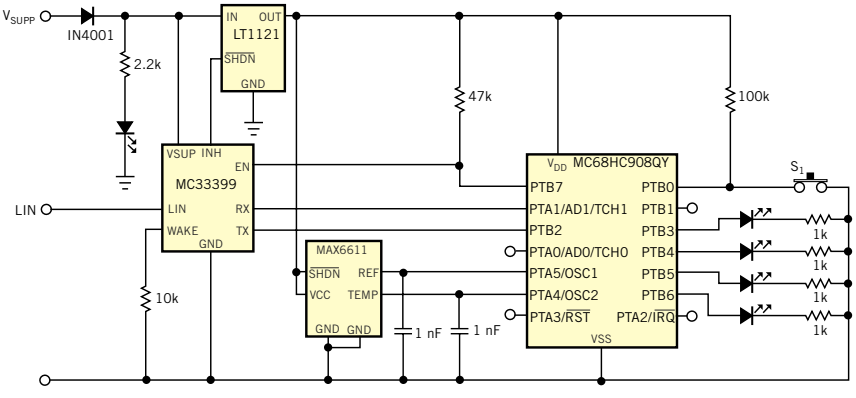

Figure 5 A reference design from Freescale illustrates a typical microcontroller-based implementation of a slave node.

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available from vendors, including almost all of the transceiver suppliers. Currently, Atmel and On Semiconductor supply only the physical-layer interface, but both companies plan to offer the protocol logic, as well. Marcel Hennrich, Atmel's marketing manager for LIN products, confirms that derivatives of the company's AVR range will include the LIN transceiver, a 5V regulator, and a system watchdog. To assist its modular-development strategy, the company will offer a LIN-protocol stack from a third-party supplier to complement its normal tool chain. At On Semiconductor, the company's automotive-applications manager, Leo Airchriedler, says that the next step is to offer a LIN transceiver with an integral voltage regulator: "We will be carefully watching the market, and, if the demand is there, we will consider integrating the protocol logic, too." This combination forms the so-called SBC (system-basis-chip).

Available SBC examples include Freescale's MC33689, which bundles the transceiver, protocol handler, and voltage regulator into a 32-pin, 0.65-mm-pitch, surface-mount outline. This chip also includes three protected high-side drivers two of which support PWM; an uncommitted op amp intended as a current-sense amplifier; two high-voltage wake-up inputs; a configurable watchdog window timer; and an interrupt output that can signal undervoltage- and overvoltage-supply problems. An SPI port enables setup from a host, including several low-power-mode and slew-rate options. The chip also includes additional hardware-protection features, such as overtemperature shutdown and overcurrent limiting.

Freescale shows some representative applications on its Web site, such as AN2623's temperature-sensor example (**Figure 5**). Here, the application runs under supervision from a 68HC908QY microcontroller with 4 kbytes of flash. The example shows the MC33399's handling the physical-layer-level translation and controlling the node's power supply by driving the Inhibit Pin of Linear Technology's LT1121 micropower low-dropout-voltage regulator. The software uses Freescale's LIN driver that is freely available from its Web site.

Freescale's Ross Mitchell says that it is just about possible to code a simple application into less memory, such as the 1.5 kbytes on the entry-level 908 family members, but considers 4 kbytes as a practical minimum. He and other vendors concur that the "sweet spot" for LIN lies somewhere around the 8-kbyte area for slaves, enabling applications such as window lifters with occupant-pinch detection. Intelligent-distributed-control chips, such as the MM908E625, employ the company's SmartMOS process to tighten integration for space-constrained nodes that require H-bridge motor control, such as headlamp levelers and mirror controllers. A new 908 family member, the MC68HC908QL4, includes an on-chip LIN-protocol handler and automatically synchronizes to the bus timing to suit slave use. The product is available now, and the company offers a $199.95 evaluation board that complements its LINkit demo boards.

According to Microchip's Stelzer, the

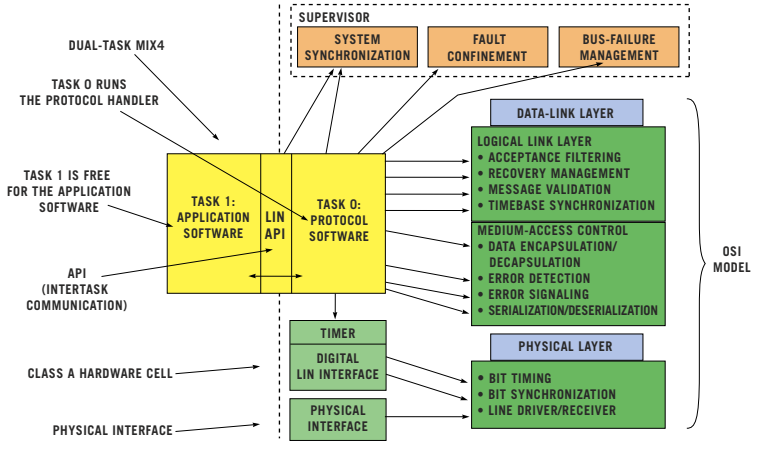

Figure 6 The MLX4 core from Melexis runs the LIN task and application software in two separate areas to emulate a two-task RTOS in hardware.

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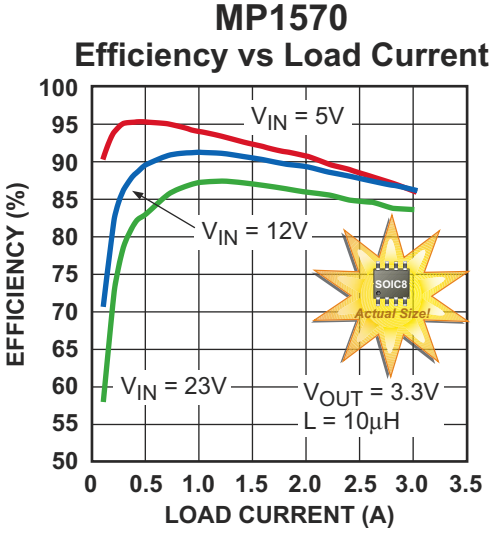

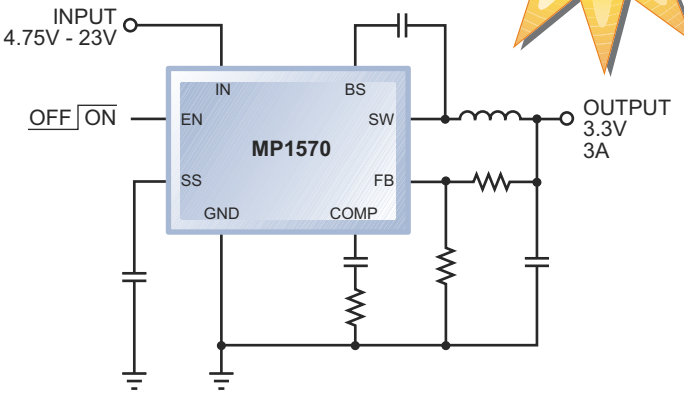

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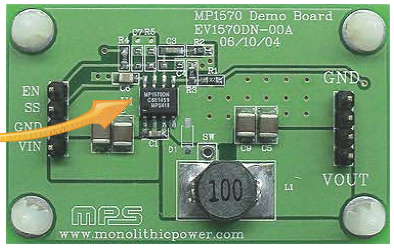
MP2106	800kHz	2.6 - 13.5	1.5	QFN10 (3x3)
MP2305	340kHz	4.75 - 23	2.0	SOIC8
MP1570	340kHz	4.75 - 23	3.0	SOIC8
Featured Non-Synchronous Bucks				
MP2361	1.4MHz	4.75 - 23	1.5	QFN10 (3x3)
MP2364*	1.4MHz	4.75 - 23	2x 1.5	TSSOP20
MP2354	380kHz	4.75 - 23	2	SOIC8
MP1593	385kHz	4.75 - 28	3	SOIC8

* *Dual Output*

MP1570 (EV1570DN-00A) Evaluation Board Available



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requirement for slaves to synchronize to the master's baud rate requires as many as 16 bits of timing resolution; hence, conventional UARTs aren't up to the job. For this reason, the company offers LIN-enhanced UARTs on chips such as its PIC16F688, which also includes features such as auto-wake-up on bus activity. This device uses the modified Harvard RISC architecture that is familiar to PIC users, and carries 4k words of program flash with 256 bytes of EEPROM for in-system-configuration data. Stelzer states that C programmers often favor higher end chips, such as the PIC18 family that provides more memory and substantially more computing power. The latest members are the PIC18F4x20/18F2x20 that offer 6 to 64 kbytes of program memory, speeds as high as 10 MIPS, and 28- and 44-pin QFN packages. They enjoy the same LIN enhancements as the F688, including Microchip's nanoWatt power-management technology that can reduce sleep-mode current drain to less-than-1-μA levels. All Microchip's LIN-slave products include on-chip RC oscillators that eliminate external resonators or crystals. For master tasks, Stelzer recommends the PIC18F4680, a 64-kbyte device with 1 kbyte of data EEPROM and the company's LIN-specific enhancements among its total of 36 I/O pins. This chip also carries Microchip's enhanced CAN interface, enabling use as a CAN-to-LIN bridge.

Melexis took a different path with its LIN-specific MLX4 core. Michael Bender, the company's marketing manager for LIN products, says that this core appears in the TH8100, a single-chip slave for intelligent-switch modules, and forms the basis of several new chips that will roll out over the coming months. The TH8100 embodies the bus transceiver and its synchronization logic, with a LIN 1.3-compliant protocol handler and internal voltage regulation that powers the chip from the 12V rail. Requiring minimal external components, it includes 17 switch inputs, three ADC channels, and three PWM outputs. Its 4-bit MLX4 core has two independent register sets that partition and simultaneously handle the LIN protocol and the application (**Figure 6**). Each task owns a private set of peripherals, such as a timer and UART, and a private memory area. Flags and mutual-exclusion logic protect intertask data transfers to prevent both tasks from simultaneously writing to the same RAM address. Because register-set switching occurs after every instruction, each task has 50% of the core's 4-MIPS capacity. The system can also dynamically share the available processing power; if one task enters wait mode, all processing power becomes available to the other task.

Additional sources of LIN-enabled hardware include Japanese microcontroller giants Fujitsu, NEC, and Renesas, as well as programmable-logic specialist such as Xilinx, and IP (intellectual-property)-core designers Intelliga and Fraunhofer Institut. LIN now appears on the 32-bit ARM platform, too, courtesy of Philips' SJA2020. Now available for sampling in a 144-pin package, this 60-MHz device carries 256 kbytes of flash and supports as many as six CAN channels and four LIN masters. Analog Devices intends to add a LIN 2.0-compliant transceiver to its ARM7-core ADμC702x series, which currently supports the protocol via a UART-based software implementation.

This widespread support suggests a bright future for a technology that is only just beginning to emerge in production applications. Issues that industry insiders are keenly monitoring include the protocol's acceptance in the Japanese market, its progress toward ISO-standard recognition, and its penetration into areas outside automotive. As Microchip's Stelzer observes, freezing LIN 2.0 was an essential step toward getting the technology into design wins. He also notes that consumer applications, such as white goods, can be even cheaper by dispensing with the 12V medium: "They can use a single-wire, 5V system, because 12V is simply an extra effort."□

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Analog Applications Journal

BRIEF

Understanding Power Supply Ripple Rejection in Linear Regulators

By John C. Teel • *Analog IC Designer, Member Group Technical Staff*

Power Supply Ripple Rejection (PSRR) is a measure of how well a circuit rejects ripple at various frequencies coming from the input power supply and is very critical in many RF and wireless applications. In the case of an LDO, it is a measure of the output ripple compared to the input ripple over a wide frequency range (10Hz to 10MHz is common) and is expressed in decibels (dB). The basic equation for PSRR, and more specifically PSRR for an LDO, can be written as:

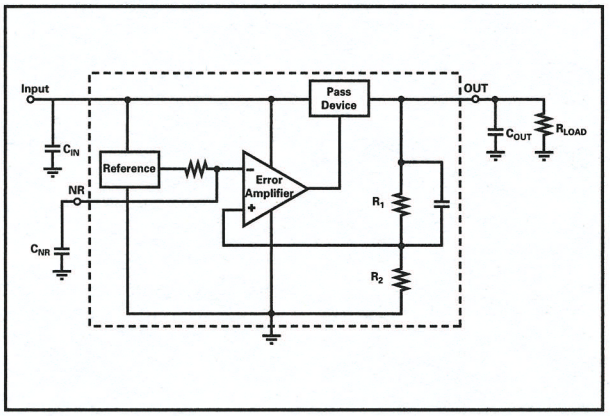
$$PSRR = 20 \log \frac{Ripple_{INPUT}}{Ripple_{OUTPUT}}$$

where A_V is the open-loop gain of the regulator feedback loop and A_{VO} is the gain from V_{IN} to V_{OUT} with the regulator feedback loop open.

$$PSRR = 20 \log \frac{A_V}{A_{VO}}$$

From this equation it can be seen that to increase the PSRR it is beneficial to increase the open-loop gain and decrease the gain from V_{IN} to V_{OUT}. Typically, A_{VO} is significantly less than 0dB with –10 to –15dB being typical and this is entirely driven by parasitics (internal and external) from input to output and at the gate of the pass-FET. Figure 1 shows a simplified block diagram of a PMOS pass-FET.

Figure 1:



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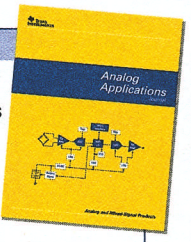
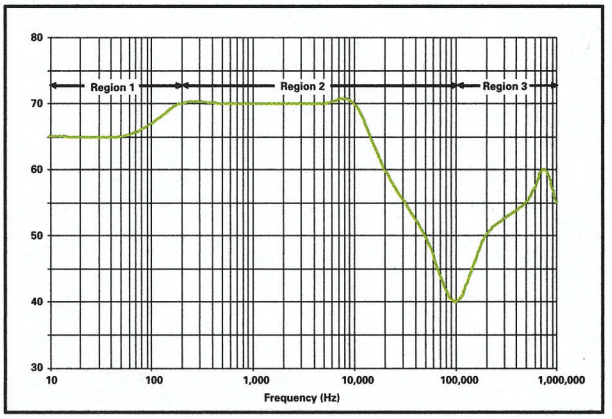


Another parameter that is closely related to PSRR is line transient response. PSRR is specified at specific frequencies, whereas a line transient essentially contains all frequencies due to the Fourier components of a step function; however, the primary difference is that PSRR is a small signal response, whereas line transients are large signal and thus are theoretically much more complicated in nature. However, what improves PSRR improves line transient response and typically vice versa (unless what improves the line transient is only a large signal improvement) so many times it is convenient to just improve one or the other knowing that both will be improved. Therefore, all of the effects on PSRR discussed in this article will also have the same effect on the line transient response.

A curve showing PSRR over a wide frequency range is shown in Figure 2.

Figure 2:



As mentioned previously the open-loop gain of the LDO feedback circuit is the dominant factor in PSRR (at least in a limited frequency range) and therefore LDOs requiring good PSRR typically have high gain with a high unity-gain frequency (large gain-bandwidth product); however, this also makes the loop more difficult to stabilize and that keeps a limit on how much the gain-bandwidth product can be increased to improve PSRR. It is important to have a high unity-gain frequency so that the amplifier does not lose open-loop gain at relatively low frequencies thus causing PSRR to also roll off.

The curve in Figure 2 shows that PSRR for an LDO can be broken down into three basic frequency regions. The first region is from DC to the rolloff frequency of the bandgap filter and is dominated by both open-loop gain and bandgap PSRR. The second region extends from the bandgap filter rolloff frequency up to the unity-gain frequency and in this region PSRR is dominated mainly by the open-loop gain of the regulator. Above the unity-gain frequency is region three and here the feedback loop has very little effect because there is no longer any open-loop gain and the output capacitor dominates along with any parasitics from V_{IN} to V_{OUT}. Also the gate driver's ability to drive the pass-FET gate at high-frequency has an effect in region three . A larger output cap with less ESR will typically improve PSRR in this region. It should be noted that although increasing C_{OUT} can improve PSRR it can also actually decrease the PSRR at some frequencies. This is because increasing the output capacitor lowers the unity-gain frequency thus causing the open-loop gain to rolloff earlier therefore lowering PSRR in that region. Although a larger output capacitor will cause the PSRR to roll off earlier, the minimum PSRR that occurs at the unity-gain frequency will typically be improved.

Anything affecting the gain of the feedback loop also affects PSRR in region two. One example is load current. As load current increases the open-loop output impedance of the LDO decreases (a MOSFET's output impedance is inversely proportional to the drain current) thus lowering the gain. In addition to lowering the gain, increasing the load current also pushes the output pole to higher frequencies thus broadbanding the feedback loop. So the net effect of increasing the load is a reduction in the PSRR at lower frequencies (because of the reduced gain) along with an increase of PSRR at higher frequencies.

Another example that affects PSRR by changing the regulator open-loop gain is the differential DC voltage between input and output. As V_{IN}–V_{OUT} is lowered less than about 1V, the internal pass-FET (which provides gain in a PMOS design) starts to be pushed out of the active region (saturation) of operation and into the triode/linear region thus causing the feedback loop to lose gain. The dividing line between the active region and the triode region is proportional to the square-root of the drain current (load current). So as the load current is increased the necessary voltage across the device (V_{IN}–V_{OUT}) to keep it in the active region increases as the square-root of load current. So, for example, having V_{IN}–V_{OUT} at only 0.5V may have no negative effect on PSRR at light load currents because the pass device doesn't need much headroom to stay in the active region so the gain is preserved. However, at heavier loads 0.5V may no longer be sufficient and the pass device will enter the triode region and the circuit will lose gain and PSRR will be reduced. When comparing PSRR among various LDOs, it's always important to compare them at identical V_{IN}–V_{OUT} and ILOAD conditions (it's also important to compare LDOs at identical output voltages since PSRR is usually better at lower output voltages).

One of the dominant internal sources of PSRR in an LDO is the PSRR of the bandgap reference. Any ripple that makes its way on to the reference will get gained up and sent to the output so it's important to have a bandgap reference with high PSRR. Typically, the solution that is chosen is to simply filter the bandgap with a low-pass filter. This way only the PSRR at low-frequencies (i.e. line regulation) is important for the bandgap thus greatly simplifying the bandgap, design because the LPF takes care of all the ripple at frequency. This LPF is almost always accomplished with an internal resistor and an external capacitor (large resistors are much easier to fabricate on-chip than large capacitors). The effect of this LPF can be seen in Figure 2 and as can be seen below the RC filter frequency (region 1), the PSRR is reduced somewhat by the PSRR of the bandgap coming into play.

As has been shown there are many things that can be done to improve the PSRR in a LDO application. The most important being to start off with an LDO designed for high PSRR such as the TPS793/4/5/6xx family of low-noise, high-PSRR LDOs and the TPS799xx low-noise, high-PSRR, low-I_Q LDO. The next most critical decision is the selection of the output capacitor with a low ESR ceramic capacitor being the best choice and the capacitance value being determined depending on at which frequencies PSRR is most important. Finally, board layout must be carefully done in order to reduce the feedthrough from input to output via board parasitics.

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Playing it Safe with Output Overload Protection

by Peter Vaughan
Manager of Product Applications
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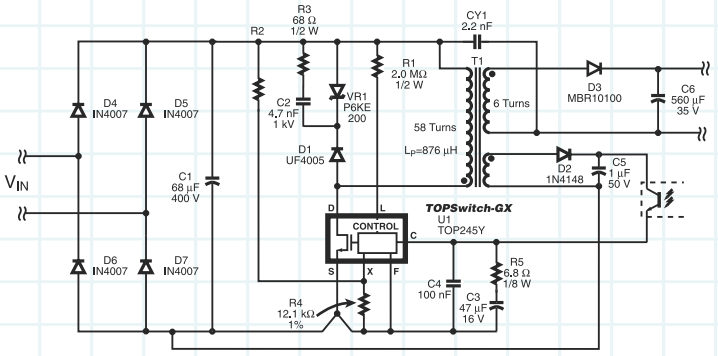
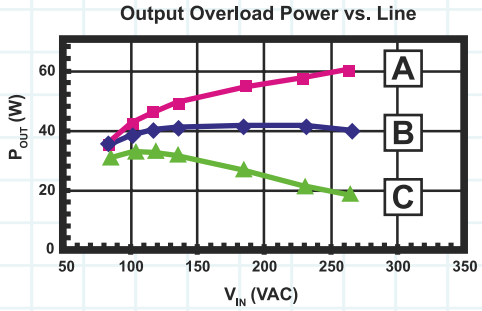
Take a break from your daily routine and test your power supply design knowledge by trying your hand at answering the three questions below regarding output overload, a stressful condition that can jeopardize the safety of your system. Then check your answers at ***www.powerint.com/puzzler2*** and enter for a chance to win a new Apple iPod Mini.

The schematic to the right shows a flyback power supply built with a *TOPSwitch*®-*GX* power conversion IC. The following questions concern the output overload characteristics of the power supply.



Input: 85-265 VAC **Output:** 12 V, 2.5 A

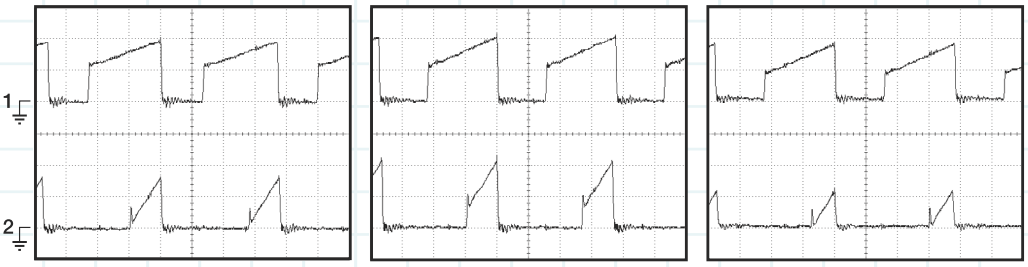
Question 1: beginner



Which of the curves in the graph to the left (A, B or C), represent the overload characteristic of output power versus input voltage for a typical flyback power supply that is not compensated for line voltage?

Question 2 : advanced

Flyback drain current waveforms* X, Y and Z were taken at 85 VAC and 265 VAC. Match the waveform pairs to curves A, B and C above.



Waveform X : ____ Waveform Y : ____ Waveform Z : ____

***Test Conditions:** Upper trace (1) V_{IN} = 85 VAC, lower trace (2) V_{IN} = 265 VAC, both traces 0.5 A/div, 2 µs/div

Question 3 : expert

It's possible to compensate the output overload characteristic of a typical flyback power supply by controlling the peak drain current limit of the converter. When using *TOPSwitch*-*GX*, compensation is achieved by correctly choosing the value of just one passive component, R2 in the schematic above. What are the advantages of achieving a flat output overload characteristic?

The answers to these questions can be found at ***www.powerint.com/puzzler2****. Check out how well you did and enter to win an Apple iPod Mini!*

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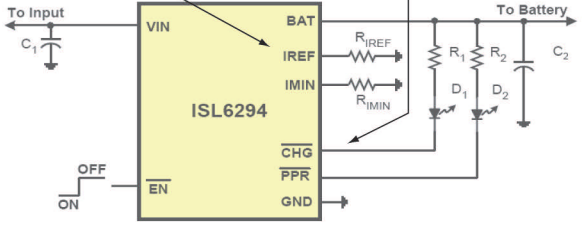
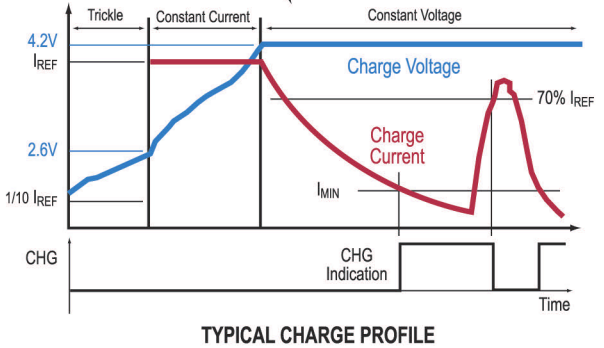
End-of-charge (EOC) current indicated through the CHG pin (which can be interfaced to a micro processor), but the charger continues to output the 4.2V.



If the battery voltage is below 2.6V the ISL6294 charges the battery with a trickle current of one-tenth of I_{REF}. When the battery voltage reaches 4.2V, the charger enters a CV mode and regulates to fully charge battery without the risk of over charge.



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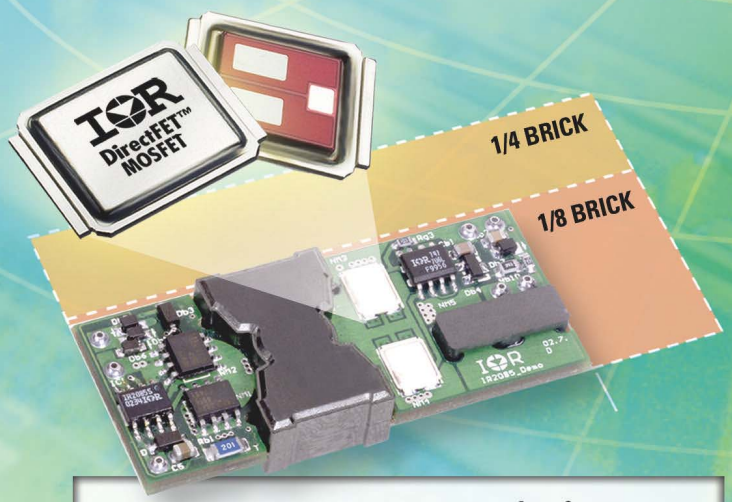

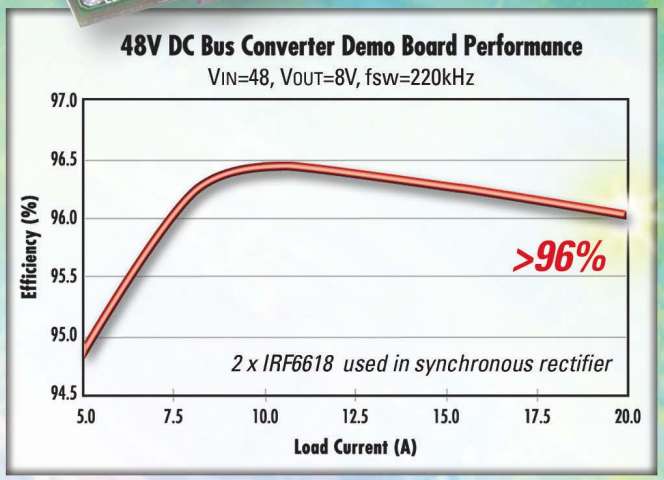

Part #	Function	BVDSS	$R_{DS(on)}$ @ 10V_{GS}	V_{GS}	I_D @ Tcase=25°C	Q_G typ.	Q_{GD} typ.	Layout code per AN-1035
IRF6618	Sync FET	30V	2.2mΩ	±20V	150A	46nC	15nC	MT
IRF6612	Sync FET	30V	3.6mΩ	±20V	89A	28nC	8.8nC	MX

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EDN 2005 DSP DIRECTORY

TARGETED DSPs TAKE AIM

DSP OPTIONS CONTINUE TO EXPAND AND ARE TARGETING OPTIMIZED CONFIGURATIONS FOR SPECIFIC APPLICATIONS. CHECK OUT THE INAUGURAL ONLINE TABLE FOR A DETAILED VIEW OF CURRENT DEVICE AND CORE OFFERINGS.

WELCOME TO THE 2005 *EDN* DSP DIRECTORY. This directory continues to grow at a substantial rate each year—so much so, that this year's edition comprises an annual update of companies and products that is available in both *EDN*'s print and online editions and a comprehensive table listing devices and cores that is available exclusively on the Web. The table presents DSP-market offerings in a dense format, highlighting the latest developments in the market and providing an up-to-date listing of current and valid processor offerings. Find it at the Web version of this article at www.edn.com, where you can also share your thoughts for making the directory even more useful as the market continues to change.

According to market-research company Forward Concepts (www.fwdconcepts.com), the DSP-chip market grew 27.2% during 2004. The wireless market accounts for almost three-quarters of that growth at 71.5% (up from 68% in 2003). It's noteworthy that most of the gains occurred in the first half of last year, because the (mostly) Chinese cell-phone makers had to deal with a glut of inventory. Forward Concepts has lowered its forecast for the 2005 DSP-market growth from 20 to 10%.

As signal-processing designs become more complex, device and IP (intellectual-property) vendors are developing and packaging bundled resources, platforms, or reference designs to demonstrate to designers how to use their products for specific applications. DSP vendors are committing serious design resources to developing reference designs, which continue to gain importance as tools to secure strategic design-in wins. These reference designs often go beyond samples and application notes—in some cases, to the point of turnkey implementations. Currently, finding a vendor's available reference designs is neither straightforward nor consistent within a company's product material. *EDN* plans to highlight reference-design information in this directory, and this year in its 2005 Microprocessor Directory, as well as in annual updates.

EDN has loosened the criteria for inclusion in the DSP directory to better accommodate the many ways to implement signal processing, including hybrid combinations of software-programmable DSPs, fixed-function devices, reconfigurable devices, and host microprocessors. Standard processor devices with multiple DSP and RISC cores and the development tools that support these devices continue to become more common. The current online table categorizes DSP offerings not by application space but rather by vendor. If you have ideas about column headings that would be more useful to your search for the perfect DSP product, please drop us a line. Likewise, if you have ideas for how to incorporate other types of signal-processing options, such as fixed-function blocks, reference designs, and platforms, please e-mail your ideas to us at dspdirectory@edn.com.

By Robert Cravotta, Technical Editor

ALTERA

Over the previous year, Altera continued to extend its programmable-logic products and tools. The Hardcopy II line of structured ASICs features an FPGA front-end design methodology; Altera built the architecture around a fine-grained collection of transistors called HCells that support the seamless migration from an FPGA to realize the density, cost, performance, and power benefits of ASIC technology. Altera also unveiled the Stratix II EP2S180 device—its largest and fastest FPGA. Version 4.2 of the Quartus II design software includes new PowerPlay power-analysis and -optimization technology. Altera's SOPC (system-on-programmable-chip) software-development tools and IP cores help designers target applications in the communications, computer peripheral, and industrial markets.

Altera maintains Web resources, including FAQs, device and IP support, design-software support, and mySupport, with which users can create, view, or update service requests and manage software subscriptions or IP licenses. The Cyclone II DSP-development kit to assists developers with wireless-infrastructure, medical-diagnostics, imaging, and test-and-measurement equipment. In addition to a development board, the development kit includes the latest version of The MathWorks' Simulink software, Altera's DSP Builder, and the Quartus II design software. Altera provides reference designs for broadcast, automotive, computing, and wireless applications that designers can use to reduce design time and improve their understanding of Altera products' capabilities.

AMI SEMICONDUCTOR

Over the previous year, AMI Semiconductor acquired DSPfactory, which focuses on the medical market, specifically in providing digital-signal processing as ASICs and standard products for ultralow-power medical wireless applications. It also introduced the Orela 4500 series, which targets DSP-based, mixed-signal audio systems to provide audio processing and exceptional sound quality for digital hearing aids that require sophisticated processing capabilities and advanced features. The BelaSigna 200 series targets high-performance DSP-based audio systems, such as wireless, industrial, and specialty headsets, and other ultralow-power, small-form-factor audio applications. AMI Semiconductor introduced bundled signal-processing algorithms for use with the BelaSigna 200, including streaming audio for wireless reception of high-fidelity stereo sound on Bluetooth stereo applications and telecom algorithms for communication in Bluetooth telecommunication headsets. The reconfigurable, DSP-based Toccata Plus system targets midrange to high-range hearing-aid applications.

AMI Semiconductor offers a suite of simulation, evaluation, development, and application tools for each of its devices. Evaluation and development kits include a board for rapid prototyping, evaluation, and testing; sample code demonstrating real-time algorithms; bundled UltraEdit advanced and integrated development editor with AMIS extensions; firmware support for developing real-time algorithms; a complete compilation-tool chain; low- and source-level debuggers; an EEPROM-manager-layout tool; and documentation. The Hybrid demonstrator board enables digital-hearing-aid developers to connect AMIS Orela 4500 series hybrids directly to transducers, switches, trimmers, and other peripherals to evaluate the real-world performance of their designs. The Advanced Headset reference design, which RF Micro Devices and AMI Semiconductor jointly developed, provides an end-to-end option for wireless streaming audio. The hardware incorporates the AMIS BelaSigna 200 DSP-based audio system with an integrated codec. Possible applications include streaming audio from a PC, notebook, portable audio player, or other analog source to a headset.

ANALOG DEVICES

The 16/32-bit Analog Devices Blackfin embedded processor targets the computational demands and power constraints of embedded audio, video, and communications applications. Based on the MSA (Micro Signal Architecture) that Analog jointly developed with Intel, the Blackfin Processor family combines a 32-bit RISC-like instruction set with 16-bit dual MACs (multiply/accumulate) units. Dynamic power management enables lower power consumption by allowing the simultaneous adjustment of system operating frequency and voltage under application control. Analog Devices' Crosscore tools support development for the Blackfin processors and consist of the VisualDSP++ development and debugging environment, EZ-kit Lite evaluation kits, EZ-Extender daughterboards, and emulators. Release 4.0 of VisualDSP++ incorporates TCP/IP and USB support, a processor configuration/start-up code wizard, and multiple-project management.

The recently available ADSP-BF534/36/37 devices are a functional extension of the ADSP-BF531/32/33 processors. The higher performance ADSP-BF537 offers more embedded memory, enabling higher throughput needs for embedded-system applications, such as video security/surveillance and industrial-environment-based distributed-control and factory-automation applications. The ADSP-BF536 targets low-cost connected devices, such as remote monitoring devices, VOIP (voice over Internet Protocol), and biometrics applications. The ADSP-BF534 processors' system peripherals include an integrated CAN (controller-area network) 2.0B controller; a two-wire interface controller; UART and SPI ports; external DMA request lines; 32-bit timers (some with PWM capability); a real-time clock; a watchdog timer; and a parallel peripheral interface. The ADSP-BF536/537 further extends these features by adding an integrated IEEE-compliant 802.3 10/100 Ethernet MAC and an enhanced DMA system for high network-bandwidth capability.

ARC INTERNATIONAL

The five-stage-pipeline ARC 600 family of configurable and extendable cores provides embedded control, computation, and digital-signal-processing tasks targeting battery-operated and cost-sensitive consumer, networking, and au-

tomotive applications. The architecture includes memory options, such as single-cycle, closely coupled memories for instructions and data, as well as configurable instruction and data caches. Multiple 32-bit ports, including main memory, auxiliary registers, and closely coupled memories support external memory access. The architecture supports BVCI- and AHB (AMBA hardware bus)-configuration options.

The seven-stage-pipeline ARC 700 family of configurable cores combines a powerful 32-bit CPU and a full-featured DSP engine in a unified architecture to target the more demanding tasks of graphics, media codecs, and packet processing. The ARC 700 architecture supports embedded operating systems, such as Linux. It also supports memory options and extends external memory access via multiple 32- or 64-bit ports. ARC 600/700 DSP extensions include 16- and 32-bit MAC and saturating arithmetic instructions with access to configurable banks of XY memory. The ARC DSPlib library of custom instructions accelerates common DSP calculations.

ARM

ARM bases its VLIW (very-long-instruction-word) OptimoDE Framework, which it launched last year, on key technology it acquired from Adelante Technologies. ARM OptimoDE Data Engines are licensable IP with an associated tool environment, a datapath functional-resource library, and preconfigured microarchitectures with varying parallelism and performance. Designers can use OptimoDE, which targets high-performance embedded signal-processing applications, as stand-alone processors or in designs with microprocessor cores. It supports parallelism, a virtually unlimited datapath configuration (including mixed widths), user extensibility, and access to fixed-function or reprogrammable data engines. OptimoDE Data Engines are compatible with ARM's DSP Interface Specification, which describes the interfaces between the cores for mailbox-based command-and-control messaging and bulk data passing, debug and trace interfaces and protocols for multicore debugging, and software APIs for interprocessor communications.

By supporting reprogrammability, the OptimoDE design process enables designers to freeze the Data Engine architecture and continue to tune the algorithm through software changes. This approach enables multiple algorithms with similar requirements to use the same Data Engine hardware. Developers can reprogram OptimoDE Data Engines once they have committed the design to manufacture or they are shipping it in volume. They can regenerate code to accommodate incremental design changes or alternative algorithms without altering the underlying hardware architecture.

The tool environment enables designers to configure and extend the type and number of datapath-resource units. Designers may also configure the size and topology of local storage and the level of interconnect. ARM provides a C compiler and profiling-analysis tools that enable designers to program OptimoDE Data Engines in C or C++. The OptimoDE tool environment automatically generates simulation models that designers can use to verify the integration process, once the data engine is incorporated within a design. OptimoDE Data Engines are AMBA-compliant and work with a variety of ARM System IP.

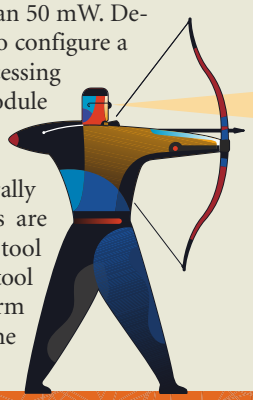
ATMEL

Atmel's high-performance, 40-bit, floating-point, VLIW Magic DSP can perform as many as 10 arithmetic operations per cycle and enable a single-cycle FFT Butterfly. It provides native support for complex arithmetic and vectorial SIMD (single-instruction-multiple-data) operations. The dual-processor Diopsis 740 device integrates a Magic DSP and an ARM7TDMI microcontroller core with 1.9 Mbits of RAM. The product targets complex-domain, floating-point, high-precision, embedded-system applications, including professional-quality audio, speech processing for hands-free phones, radar-based automobile-collision avoidance, acoustic diagnosis of mechanical equipment, and software-based ultrasound scanners.

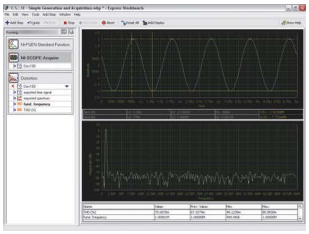
Over the previous year, Atmel has added features to the MADE (multicore-application-development environment) debugging capabilities. MADE, the Diopsis integrated development environment, includes C compilers for both ARM and Magic DSPs, a high-level Magic DSP macro-assembler/optimizer, an eCos RTOS, a library of C-callable DSP functions, and a unified debugging environment interfacing with a cycle-accurate simulator or a Diopsis board. The C-callable DSP library has grown from 75 to 125 functions. The library includes a variety of FFTs, IIRs, and FIRs on single-sample sequences or input-data streams; vectorial square roots; vectorial magnitudes; and vectorial arithmetic and trigonometric operations, and a rich set of matrix functions. Atmel also introduced two boards for the Diopsis DSP—the Test and Evaluation Board and a Dual Diopsis PCI mezzanine card.

CAMBRIDGE CONSULTANTS

Cambridge Consultants' configurable VLIW APE2 DSP targets adaptive datapath signal-processing applications. The company based it on a software-DSP-generator tool kit. APE2 targets consumer-market applications such as wireless, audio, and measurement systems by minimizing silicon cost and maximizing performance. For example, an APE2 configured for a hearing-aid application requires fewer than 20,000 gates and consumed less than 50 mW. Designers use the generator tool kit to configure a VLIW DSP from ready-to-use processing elements it draws from the APE module library together with dynamic datapath routing. The starting point for algorithm design is generally Matlab, and the same operations are simulated using the APE software-tool kit. Once the system is working, the tool kit produces an APE2 DSP in the form of a Verilog netlist, together with the



NI LabVIEW – From Interactive Measurements to Graphical System Design



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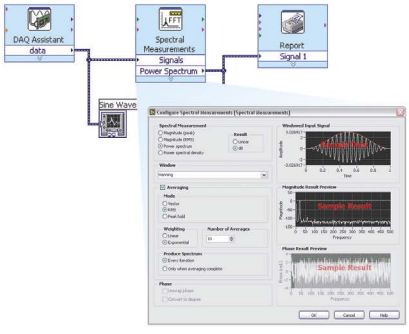

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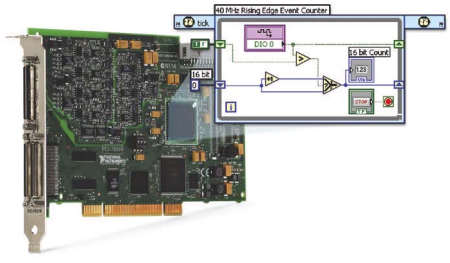

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assembly language to run the signal-processing task.

During the previous year, Cambridge Consultants extended the range of APE2 processing modules for math-intensive operations with trigonometric, vector, ratio, reciprocal, coordinate-transform, square-root, exponent, and logarithmic functions. These modules complement the MAC, ALU, radix-4 FFT, sequencing, I/O registers, and memory-interface modules that were already available. Designers can license the software-tool kit and transfer the APE2 technology into their teams. Alternatively, Cambridge Consultants can analyze a design's requirement and produce a silicon-ready APE2 IP core for integration into a licensee's ASIC project. APE2 license fees have no per-chip royalty.

CEVA

Last year, Ceva announced the Ceva-X architecture framework, a scalable VLIW-SIMD DSP architecture targeting baseband and multimedia applications, such as 3G multimedia phones, PDAs, digital cameras and camcorders, DTV and high-definition DVD. The first implementation of the Ceva-X family, the Ceva-X1620, combines microcontroller and signal-processing functions in a variable-width (16/32-bit) instruction set. The Ceva-X1620 can simultaneously issue as many as eight instructions and offers high code compactness using SIMD concepts. The Ceva-XS1100 and Ceva-XS1200 are new complete systems built around this DSP architecture that include peripherals, interconnections, and interfaces to external memories, I/Os, and CPU systems. The Ceva-XS1100 and Ceva-XS1200 are two DSP subsystems built around the Ceva-X1620 DSP. These subsystems include a 3-D DMA coprocessor to better target multimedia applications. The Ceva-XS includes interfaces to Level 2 memories, APB peripherals, and a CPU system based on 64-bit AHB-Lite master/slave ports.

Ceva announced the Mobile-Media, a DSP-based multimedia platform that consists of a DSP core (based on Ceva-Teak or Ceva-X), a DSP subsystem (Xpert-Teak or Ceva-XS), and a set of optimized software modules that target the mobile multimedia market. The 16-bit-fixed-point, general-purpose Ceva-Teak DSP core features a dual-MAC architecture for complex signal processing. It includes built-in accelerators for FFT and Viterbi to target portable-multimedia and wireless-communication applications. Ceva built the Xpert Teak subsystem around the Ceva-Teak dual-MAC DSP core; it includes a power-management unit, an interrupt controller, general-purpose I/Os, timers, on-chip emulation, TDM ports, and a code-replacement unit. It also includes a 3-D DMA engine to support multimedia applications through video-related data transfers.

Ceva's fully programmable Mobile-Media platform supports H.264 encoding and decoding at full D1 resolution, 30 frames/sec, without any hard-wired acceleration. Other than the H.264 codec, Mobile-Media includes MPEG4, H.263, JPEG, and AAC codecs. Other audio codecs, such as MP3, WMA, AAC+, and AMR, are optional. Ceva also announced the Ceva-TeakLite-II, a revved-up DSP architecture based on its predecessor, the Ceva-TeakLite, to target 2G/2.5G handsets and optical-disk applications. Other improvements to the architecture include increased memory space and a higher level of system integration.

CHIPWRIGHTS

Fabless semiconductor company ChipWrights offers video-processing technology to reproduce lifelike imagery in mobile personal-entertainment products, digital video/digital still "dual cams," and high-demand video applications, such as security cameras and digital television. The new ChipWrights CW5521 SIMD processor combines a RISC processor, a parallel processor with 16 32-bit datapaths, enhanced video-sensor features, USB, audio-codec compact flash, and secure digital-card interfaces.

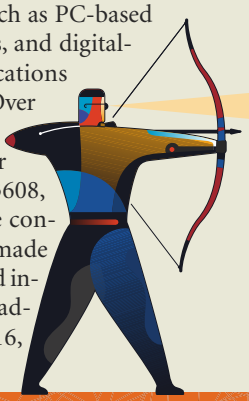
The ChipWrights development environment includes a software-development kit that integrates a compiler, a simulator, a profiler, a linker, and a debugger into the Metrowerks CodeWarrior integrated-development environment. The Reference Application Specific Libraries include resources for image processing, video and audio codecs, a ChipWrights BIOS, and development boards.

CIRRUS LOGIC

Cirrus Logic's 32-bit CS4961XX family features an audio systems processor that integrates a DSP with dual MACs; dual memory moves; dual index registered update; and log/exp assist. Optimizations for butterfly FFT, FIR, and IIR with CobraNet technology deliver uncompressed digital audio over Ethernet networks. Cirrus Logic supports a library of audio algorithms, including THX Ultra2, DTS ES 96/24, Dolby Surround Pro Logic IIx, and a modular programming environment for easy customization. Cirrus Logic introduced the Intelligent Room Calibration software for automatic speaker setup and room equalization using its CS495XX and CS494XX DSPs. The framework includes state-of-the-art decoders, virtualizers, surround simulators, and audio-enhancement algorithms. Cirrus Logic's DSP A/V-receiver reference design includes a library for firmware feature differentiation.

CRADLE TECHNOLOGIES

Cradle's 32-bit CT3000 family of programmable DSPs targets media-processing applications with a focus on video-surveillance applications, such as PC-based and embedded DVRs, IP streamers, and digital-video cameras. Other target applications include imaging and broadcasting. Over the previous year, Cradle introduced the CT3600 multiprocessor DSP family, comprising the CT3608, CT3612, and CT3616. Each device consists of two computational quads made up of processing cores, local data and instruction memory, and separate address and data buses. In the CT3616,



the family's highest performing member, each quad consists of eight single-issue pipelined DSP cores and four simple RISC-like general-purpose processors. A three-tiered memory hierarchy increases performance predictability and scalability. Each quad includes 128 kbytes of shared data memory and 32 kbytes of instruction cache, which the four general-purpose processors share. Each DSP has its own local instruction memory- and data-register file that enables the cores to run fairly autonomously. The family provides an I/O subsystem consisting of 18 programmable 8-bit pin-groups that can support interfaces including video (CCIR601/656), audio (PCM), 10/100 Ethernet, and IDE. This family provides a DDR-SDRAM interface.

The CT3600 family uses the same multiprocessor DSP architecture as the CT3400, but it supports program execution at 1.5 times the operating frequency and can include twice as many computational elements. Power consumption is 1 to 5W depending on device size, application, and operating frequency. The DSP instruction set supports special video and imaging instructions. The SAD (sum-of-absolute-difference) instruction accelerates the processing of motion estimation, and the PIMAC (packed-integer-multiply-accumulate) instruction can perform 16 8-bit MACs in a single cycle.

DSP ARCHITECTURES

This year, DSP Architectures began offering the full military version of the MILDSP24 and MILtMMU24 general-purpose signal processors. These products support extended-temperature and 75-MHz operation, which is higher than the commercially available 65-MHz DSP24. DSP Architectures has implemented a program to offer commercial (DSP24), military (MILDSP24), and rad-hard (RHDSP24) silicon cores for customer-proprietary designs.

The high-performance DSP24 vector-processor chip and its associated IP cores for signal and image processing in the frequency domain target applications that perform operations on large arrays of data. It is a pass-based processor, with each function valid for one complete pass. Each operation code defines a basic flow for the desired operation that repeats for multiple pairs of data to complete one pass. For typical array-processing applications, such as FFTs, the device sets up a function code (for example, BFLY32). Radix32 butterfly and then clocks the whole data array into the DSP24 and applies the function to it. Latency occurs when you implement the DSP24 functions, which the MMU24 automatically compensates for when you use it in a system. The pipelined systolic structure allows you to cascade multiple DSP24s for increased performance and higher radices. This structure permits high-speed operation on an unlimited array size with support for enhanced read-only FFT, double-length FFT, dual FFT, and stacked FFT to reduce latency.

EQUATOR

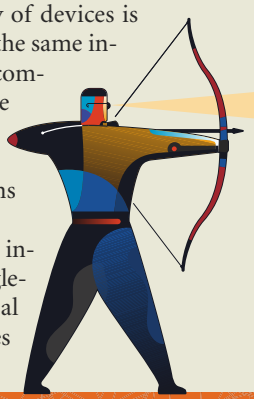
Equator's MAP series of video-centric processors, which includes the MAP-CA, BSP-15 and the BSP-16 processors, performs the central functions of digital imaging, communications, and media applications as software. The BSP-16 device is the newest member of Equator's BSP (Broadband Signal Processor) family, which includes the DataStreamer DMA engine, an onboard IDE controller, and Ethernet MAC, all operating as fast as 500 MHz. The VLIW BSP-16 CPU performs computationally intensive numeric and multidimensional matrix operations in video- and signal-processing operations. It can run video- and image-processing algorithms, operating systems, network stacks, middleware, virtual machines for Java, and Internet browsers.

The iMMediaTools software-development-tool kit consists of a suite of software tools, device libraries, and utilities for creating and optimizing video-centric applications. It features a VLIW tool chain with an ANSI C/C++ compiler; drivers to implement advanced video features, such as PIP (picture in picture); native support for Linux; Windows CE drivers; support for optimized audio and video performance from C/ C++; a multiformat media-player infrastructure that supports trick play, PIP window, and graphics overlay; GDB source-level debugging; and an operating-system abstraction layer for codecs, application code, and player/recorder infrastructure.

Over the previous year, Equator introduced cost-reduced reference designs, including the Starfish and Babelfish set-top-box reference designs. The company expanded the platform's support for audio- and video-software codecs to include Windows Media Advance Profile, H.264, RealVideo, and aacPlus. The platform also includes support for additional conditional-access and DRM (digital-rights-management) capabilities, such as Windows Media DRM 10. Equator hardware reference platforms also include reference designs targeting IPTV (Internet Protocol television), digital home and consumer electronics, security/surveillance, and videoconferencing.

FREESCALE

This year, Freescale introduced the MSC71xx family of DSPs, basing it on StarCore technology, with a DDR-SDRAM controller. This family of devices targets enterprise VOIP, IP PBX (private-branch-exchange), and network-edge and -access applications scaling from four to hundreds of channels in fractional or multiple T1/E1 increments. The family varies by peripheral sets, with the MSC7116 and MSC7113 targeting developers of Ethernet-only equipment. The MSC711x family of devices is pin-to-pin compatible and offers the same instruction-set and binary software compatibility with Freescale's StarCore technology-based MSC81xx family. It also provides Ethernet, DMA, and TDM communications peripherals.



The MSC81xx family of devices includes both high-performance single-core and multicore digital-signal processors. The single-core devices

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MSC8101 and MSC8103 and the multicore devices MSC8102, MSC8122, and MSC8126 are all software-compatible. Both product lines target computationally intensive infrastructure DSP applications, including packet telephony, media gateways, multichannel modem banks, and third-generation wireless systems. The newest devices, the MSC8122 and MSC8126, are available with 300-, 400-, and 500-MHz core speeds, and Freescale bases them on 90-nm-process technology. The MSC8122 and MSC8126 can deliver 8000 DSP MMACS at 500 MHz, yielding an effective performance equal to 2 GHz.

Freescale also announced the addition of a 275-MHz speed to the DSP56321, a member of the DSP563xx family that can perform 550 MMACS when its Enhanced Filter Coprocessor is in use. This device maintains the same full temperature qualification of −40 to +105°C as its predecessors. Freescale's 24-bit, floating-point-architecture DSP563xx processor family targets wireless and wireline infrastructure and communications equipment, as well as packet telephony, professional audio, scientific test and measurement, industrial control, and healthcare related medical equipment. This family includes the DSP56321, DSP56311, DSP56L307, DSP56309, DSP56303, and DSP56301.

Freescale also introduced the 56F8100 series of devices for price-sensitive industrial and consumer applications. It bases the series on the 56800E hybrid digital-signal-controller core, which integrates the instruction set of a DSP with the control functions of an embedded microcontroller in a single core. The 56800 family targets applications that traditionally use 16-bit microcontrollers but also require DSP functions, such as point-of-sale and voice-recognition applications, digital-telephone-answering devices, motor-control systems, and applications requiring voice, audio, or data processing.

Freescale's CodeWarrior tool suite from Metrowerks, including the SmartDSP operating system and CodeTest software-analysis tools, provides development support for all of these processor families. Freescale's Smart Packet Telephony Hardware Reference Design is for small- to large-scale media-gateway equipment capable of voice, fax, or modem data services. System architects may use this evaluation platform to assess the capabilities of Freescale's DSPs for voice compression and echo cancellation. Trinity Convergence provides the VeriCall software framework to provide a flexible, open architecture for VOIP designs based on Freescale's MSC711x and MSC81xx family of DSPs, the PowerQuicc family of integrated communications processors, PowerPC host processors, and C-3/C-5 network processors.

HYPERSTONE

Hyperstone's HyNet32S, a scaled-down version of the HyNet32XS networking processor, features the same E1-32XSR RISC/DSP core but adds PCI bus functions. Hyperstone builds the HyNet series of networking processors around the E1-32XSR core and adds integrated peripherals supporting high-speed communications (Ethernet, Real Time Ethernet, Serial, ATM), additional internal RAM, video interfacing, PCI support, DMA, and more. These processors target applications requiring high-speed signal processing; communications, including real-time Ethernet; or both.

Hyperstone's E1-16XSR/32XSR RISC/DSP processors provide seamless integrated RISC/DSP functions for any application requiring a high-speed microprocessor coupled to a high-performance DSP. These processors feature dual execution units (RISC/DSP) in a pipelined architecture sharing the same registers. Developers can transparently mix RISC- and DSP-specific programming. Devices execute RISC/DSP instructions with a high degree of parallelism, resulting in high throughput. Typical target applications for use are telephony, video, digital cameras, general signal processing, and more.

Hyperstone offers hardware- and software-development tools, including a real-time kernel, a C compiler, an assembler, a linker, an EPROM formatter, a source-level debugger, and several hardware target boards. Also available is the HyNetOS full-featured operating system, which includes a collection of communication-protocol stacks, including real-time Ethernet; a file system; and memory management. Hyperstone is also offering an application-specific hardware target board for use in the development of real-time Ethernet applications, such as Ethernet Power Link.

LSI LOGIC

The ZSP Products Division of LSI Logic is a licensor of signal-processing cores and products. LSI Logic also offers standard product offerings for lower volume designs and prototype implementations. The ZSP processor architecture targets 3G wireless handsets, multimedia, and networked voice appliances. ZSP Solution Partners augment the technology with software tools, EDA-modeling support, and a portfolio of application software. Over the previous year, the ZSP Products Division expanded its signal-processor family to include the ZSP-540 licensable core, the less-than-$4 (high volumes) LSI403LC standard product, and the off-the-shelf, bundled silicon/

software Z.Voice-729 package for VOIP applications.

The high-performance, power-efficient, quad-MAC, six-ALU ZSP540 DSP core delivers 1.2 GMACS on a 0.13-micron process. The ZSP540 core includes the Z.Turbo technology for application-specific acceleration targeting 2.5/3G baseband processing, multimedia wireless/mobile devices, WLAN, and VOIP applications. The LSI403LC DSP targets cost-sensitive applications requiring low power consumption and can gluelessly interface to popular microprocessors. Its large on-chip memory eliminates the need for external memory. ZSPneo, a new entry point to the ZSP road map, targets cost-sensitive applications that require control processing beyond 8- and 16-bit-microcontroller performance but cannot tolerate the cost and overheads associated with a 32-bit microcontroller. ZSPneo also targets one- or two-channel VOIP, audio players, speakerphones, wireless application processors, toys, and servo and vehicle controls.

LSI Logic's DSE (DSP Solutions Engineering) team, a worldwide network of DSP systems experts, provides direct consultation, training, application notes, bulletin boards, and access to the KnowledgeBase FAQ database. DSE works with ZSP Solution Partners to develop reference designs and sample systems in the form of boards, RTL, and SystemC models.

MICROCHIP

Microchip this year released to production 15 devices in the dsPIC30F DSC (digital-signal-controller) family. The two sensor devices target space-constrained applications with package options as small as 6×6 QFN. The nine general-purpose devices support a range of flash-program-memory sizes from 24 to 144 kbytes. The four motor-control/power-conversion devices feature a PWM and an ADC. Microchip also introduced a series of application libraries, including noise suppression, echo cancellation, speech recognition, and encryption that designers can evaluate for a $5 license fee.

Microchip's dsPIC30F DSC, a 16-bit modified Harvard machine, combines the control advantages of a microcontroller with the computation speed of a fully implemented DSP in a single-chip, single-instruction-stream architecture. All dsPIC30F DSCs execute from flash program memory and feature a familiar microcontroller architecture and design environment. The dsPIC DSCs feature flash memory, EEPROM, software stacks, a strong interrupt structure, mixed-signal capability, low-pin-count options, and real-time emulation. The dsPIC DSC also features dual-operand fetches, a barrel shifter, zero-overhead loops, and single-cycle 16×16 MAC with twin 40-bit accumulators.

The dsPIC30F tools operate seamlessly within Microchip's Mplab integrated development environment, a free tool suite that includes the Mplab ASM30 assembler and the Mplab SIM software simulator for writing and testing dsPIC30F code. Also available is the dsPIC30F Visual Device Initializer. A full-featured 60-day demo of the Mplab C30 C compiler is available in a download. Hardware tools include the ICE4000 Emulators, ICD2 in-circuit debuggers, and programmers to assist with in-circuit serial programming. Third parties have extended their lines of embedded cross-compilers to cover the dsPIC30F devices.

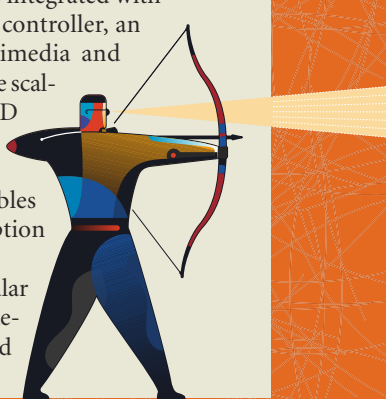
MORPHO TECHNOLOGIES

Morpho Technologies' MS1-16, an optimized rDSP IP core, targets high-performance wireless-infrastructure and power-optimized mobile devices, such as multimode wireless base stations and multimode 3G wireless handsets. The cores are optimized for the baseband-processing requirements in wireless standards. The M-rDSP architecture combines the power of a software-programmable, 32-bit RISC processor (mRISC) and an eight- to 64-cell reconfigurable cell array. Each reconfigurable cell contains an ALU, a MAC, and logic units, as well as specialized functional units that designers can use for wireless applications. The reconfigurable cell array can switch from one application-specific set of instructions to another in one clock cycle. For 3G wireless chip-rate processing, each reconfigurable cell contains a complex-correlator unit as a specialized functional unit.

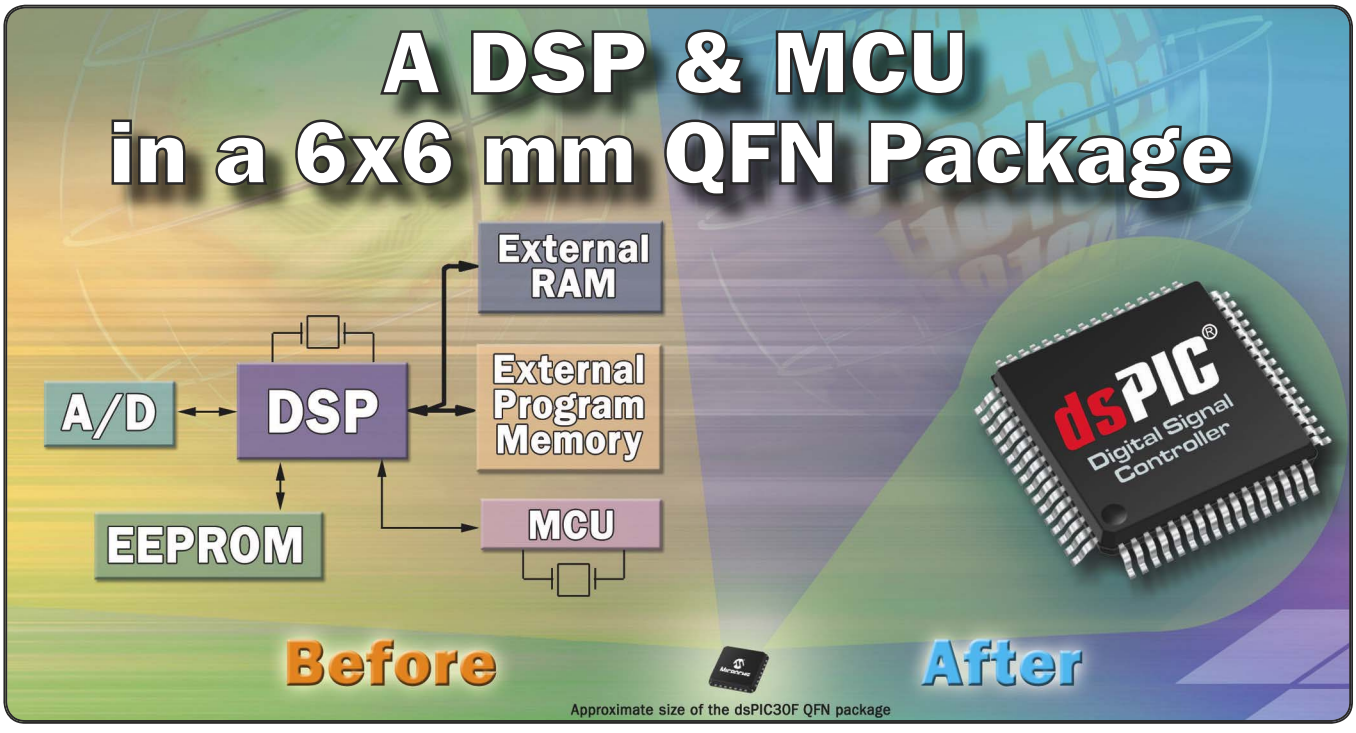
Morpho has mapped optimized software-kernel libraries, based on various communication algorithms, into its M-rDSP core and provides reference-software applications that demonstrate communications protocols and standards. Morpho provides a fully synthesizable core, a C++ cycle-callable simulation model of the M-rDSP Core, synthesis scripts/test benches, a "C" compiler, a simulator (bit accurate/cycle accurate), a library of preoptimized kernels, debugging tools, and detailed documentation. It offers hardware-development systems and software tools that it bases on a proprietary software-tool chain that follows the most commonly used and understood tools in the market today.

PHILIPS SEMICONDUCTORS

The PNX1700, the newest member of Philip's Nexperia family of media processors, targets connected multimedia products, such as IP set-top boxes, digital-media adapters, personal video recorders, videophones, and televisions. In addition to having high-definition video capabilities, the PNX1700 connected media processor doubles the performance of previous generations, and maintains hardware and software compatibility. It features a 500-MHz, 32-bit, superpipelined TriMedia CPU core integrated with a TFT (thin-film-transistor) LCD controller, an Ethernet 10/100 MAC, and multimedia and floating-point instructions for image scaling, advanced deinterlacing, and 2-D graphics acceleration. The PNX1700 supports dynamic frequency and power management that enables designers to tailor power consumption to the application requirements.



Philip's Nexperia PNX5220 cellular multimedia baseband, with dual Adelante 16-bit RD16024 DSP cores and



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dsPIC30F3010	28	24	1024	0	4/2	1	1	0
dsPIC30F3011	40/44	24	1024	0	4/4	2	1	0
dsPIC30F3012	18	24	2048	0	2/2	1	1	0
dsPIC30F3013	28	24	2048	0	2/2	2	1	0
dsPIC30F3014	40/44	24	2048	0	2/2	2	1	0
dsPIC30F4011	40/44	48	2048	0	4/4	2	1	1
dsPIC30F4012	28	48	2048	0	4/2	1	1	1
dsPIC30F4013	40/44	48	2048	AC97, I²S	4/4	2	1	1
dsPIC30F5011	64	66	4096	AC97, I²S	8/8	2	2	2
dsPIC30F5013	80	66	4096	AC97, I²S	8/8	2	2	2
dsPIC30F6010	80	144	8192	0	8/8	2	2	2
dsPIC30F6011	64	132	5144	0	8/8	2	2	2
dsPIC30F6012	64	144	8192	AC97, I²S	8/8	2	2	2
dsPIC30F6013	80	132	6144	0	8/8	2	2	2
dsPIC30F6014	80	144	8192	AC97, I²S	8/8	2	2	2

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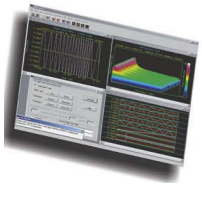

Looking to add noise suppression, encryption, acoustic echo cancellation or speech recognition to your application? These libraries and others are available now for the dsPIC30F devices with a $5.00 license fee for evaluation or development, and a low one-time fee for production.

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an ARM926 subsystem, targets feature-rich mobile handsets and smart-phone applications. It supports quadband 850-, 900-, 1800-, and 1900-MHz operation for GSM, GPRS, and EDGE and dual-band operation for UMTS. One DSP core handles the communication modem, and the other core performs the advanced audio features. Audio-processing support includes 64-voice stereo polyphony, enhanced AAC+ codecs, MP3 decoding, and wideband speech processing. Baseband-processing support includes a full software EDGE receiver and up to class 123 and SAIC (single-antenna interference cancellation). The Nexperia PNX5220 uses the 208-MHz ARM926 subsystem with hardware accelerators for application processing.

The PNX5220 memory architecture for the baseband processing uses multiple parallel buses to support NAND flash, SDRAM, cellular RAM, and burst-mode/page-mode memory. The ARM9 processor core uses a multilayer AHB structure to separate slow external peripherals from fast external memories to optimize the interaction with on- and off-chip memories. The PNX5220 has built-in Java acceleration and uses independent processing units as bus masters to enable the functional units to form a balanced network. The PNX5220 runs video at 30 frames/sec in CIF resolution and provides the hooks for GPS and other connectivity functions, such as WLAN and Bluetooth. It also allows the phone to connect via mobile connectivity standards, such as USB OTG (on the go) and fast IrDa.

The Philips' Adelante DSP technology includes the 16-bit RD1602x DSP core family and the 24-bit RD2412x DSP core family with a user-definable VLIW architecture. The RD16024 is the newest 16-bit programmable DSP core. The 24-bit Philips' Adelante RD24121 DSP core, with its 56-bit accumulator size, has an advanced instruction-set architecture suitable for audio applications requiring a high dynamic range. This architecture enables designers to trade between performance and operating voltage to enable lower power operation. The RD24121 includes an eight-stage pipeline with an orthogonal-register-file approach beneficial for the C compiler.

The Adelante software-development kit for multicore SOC architectures includes a graphical front-end with access to the underlying tool components, such as the compiler, assembler, linker, simulator, emulator, and profiler. It also offers a standard DSP firmware library with a set of DSP-related functions, such as FFT, FIR, and geometric functions. Philips makes available an FPGA-mapping of the DSP core and subsystem.

RC MODULE

RC Module bases its NeuroMatrix NM6403 DSP family of dual-core application-specific DSP processors on the NeuroMatrix Core. It targets video-image processing, radio-navigation, and radar applications and provides scalable performance by employing a programmable operand width of 1 to 64 bits; this flexibility allows designers to trade precision for performance. The NM6403 processor includes a 32/64-bit RISC processor and a 1- to 64-bit vector coprocessor that supports vector operations with elements of variable bit lengths.

This year, RC Module introduced a new software-development kit for the NeuroMatrix NM6403 RISC/DSP processor. The NM-SDK Version 2.0 includes an optimizing C++ compiler (ISO/IEC 14882:1998 standard) and real-time DSP and video-image processing libraries. The compiler more closely adheres to the C++ standard, including templates, and uses the enhanced optimizing algorithms that allow increasing program execution speed and decreasing code size. The assembly language has an intuitive syntax and is close to high-level languages so it can simplify the development and understanding of source code for math-intensive real-time algorithms.

The MC2301 PCI digital-signal memory-evaluation board targets high-frequency analog-signal processing, complex high-frequency analog-signal generation, and DSP software/hardware prototyping and development. The MC2301 has one 1879BM3 DSM SOC, a 64-Mbyte SDRAM bank, analog input and output buffers, and a PCI-host interface. The shared memory is accessible for reading and writing both from the digital-signal memory chip and from the PCI bus. The MC2301 features a programmable 128-bit on-chip controller; a DSP core; 2-Mbit on-chip SRAM; two 600M-sample/sec, 6-bit ADC inputs; two 600M-sample/sec, 8-bit DAC outputs; and 64 Mbytes of onboard SDRAM.

SENSORY

Sensory's RSC family of devices performs recognition, speech synthesis, and general-purpose product control. The RSC line includes a 16-bit ADC, a 10-bit DAC, an alternative PWM output amplifier, 128 kbytes of on-chip ROM, 4 kbytes of on-chip RAM, comparators, timers, and general-purpose I/O. The RSC-4x provides on-chip integration of features, including a microphone preamplifier, twin-DMA units, vector accelerator, hardware multiplier, timers, and 4.8 kbytes of RAM. You can build a complete system with little more than a battery, a speaker, a microphone, and a few resistors and capacitors. Multiple ROM options are available.

Over the previous year, Sensory introduced FluentChip firmware, which enables higher accuracy, larger vocabularies, improved speech compression, better trigger-word detection and rejection, more noise tolerance, improved speaker-dependent recognition performance, and more instruments for music. The RSC line supports speaker-independent recognition, speaker-dependent recognition, speaker verification for voice biometric security, speech compression for speech playback (high-quality, 2400-bps compression), and music synthesis at no additional cost.

The RSC programming and debugging tools include the Phyton macro assembler, a C compiler, and an in-

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circuit emulator, all running in an integrated development environment. Hardware demonstration and evaluation boards are available for testing and prototyping. The speech tools include Sensory's QuickT2SI speaker-independent recognition-set development tools and QuickSynthesis speech compression for playback of voice files.

STARCORE

StarCore develops and licenses the StarCore processor architecture to OEMs and semiconductor suppliers as a family of fully synthesizable cores and subsystems. The StarCore subsystems provide scalable performance across a range of communication, wireless, and multimedia applications. They include a complete set of subsystem IP blocks, such as memory controllers, an interrupt controller, and an accelerator interface to reduce development time. The design is fully synthesizable, making it readily transferable from one foundry to another as market and product needs change.

StarCore has expanded the SC1000 instruction set to include video-processing instructions, improved code density, and enhanced RTOS support for mobile multimedia applications, such as smart phones, digital still cameras, and digital camcorders. StarCore also offers the SC2000 family, which is fully binary compatible with the SC1000 series of products, for video and portable multimedia. The two-MAC SC2200 and four-MAC SC2400 include dedicated video-processing instructions, additional RTOS support, improved code density, and improved power consumption. The SC2400 family of processors offers a 60% improvement in multimedia performance over the SC1400 family of processor products.

The SC2200 and SC2400 processor cores are available in synthesizable Verilog RTL. The SP2201 and SP2401 subsystems support embedded applications, featuring enhanced multimedia performance with on-chip emulation, memory interfaces, a DMA interface, an AHB-compliant system bus-interface, a clock-control unit, and an interrupt-control unit. The SP2202 and SP2402 subsystems support advanced applications, including all the features of the SP2201 and SP2401 subsystems, plus data- and program-cache controllers, a memory-protection unit, and a high-speed interface to connect application-specific accelerators.

STMICROELECTRONICS

STMicroelectronics' new ST140 quad-MAC DSP core extends the ST122 dual-MAC implementation of the ST100 architecture that targets cellular-phone-infrastructure applications. The ST140 DSP is available as soft IP or hard macros, and it includes Viterbi-specific instructions and the ability to support user-defined operators. STMicroelectronics can map the core in various technologies and offers it with a full set of interfaces, peripherals, and memory IP. The architecture maintains software legacy between both cores and emphasizes the C ST100 compiler technology to benefit from a high level of processing parallelism directly from C source code.

The development environment supports modeling, profiling, optimizing, and debugging for any ST140-based application, including multicore designs. The STMicroelectronics technical-support team provides on-site training and brings day-to-day dedicated support to customers.

TENSILICA

Tensilica's configurable, extensible, and synthesizable Xtensa LX processor core enables designers using the Tensilica processor-generator tool to build Xtensa LX processors that exactly fit the target task. The designer selects and configures predefined processor attributes and, by using TIEs (Tensilica Instruction Extensions), adds Verilog descriptions of execution datapaths, I/O ports, and registers that can deliver performance, area, and power characteristics equivalent to custom-logic design. Over the previous year, Tensilica introduced the Xpres compiler, which can analyze the designer's C/C++ code and automatically suggest and generate the TIE instructions to optimize the processor for the application.

Tensilica's Xtensa LX processor core with Vectra DSP engine supports wide datapaths and traditional DSP tasks. The system can deliver RTL-equivalent I/O through a ports- and queues-mechanism that directly connects to the processor's execution unit to bypass the load/store operation. The Vectra LX DSP engine takes advantage of the Flix architecture and uses 64-bit instruction words containing three issue slots for ALU, MAC, and load/store operations. Tensilica offers Web-based design support and an FPGA-based development board and can customize the Vectra LX DSP engine on a consulting basis.

TEXAS INSTRUMENTS

Texas Instruments' 90-nm, 1-GHz TMS320C6414T, C6415T, and C6416T DSPs target audio, speech, video, and imaging applications. Also new is a 720-MHz version of the TMS320DM642 DSP-based digital-media processor targeting consumer electronics and set-top boxes. The DM642 delivers high-definition video streams in Microsoft's WMV HD (Windows Media Video high-definition) at 720-pixel resolution and processes standard-definition video decoding for the H.264 format. The new TMS320R2811 and R2812 digital-signal controllers target industrial, automotive, sensing, flow metering, and e-metering applications by providing 20k words of on-chip SRAM and allowing developers to add unlimited external memory to their designs via the SPI port. They include an integrated high-speed, multichannel, 12-bit ADC to measure system parameters and respond quickly to meet the input- and output-intensive requirements specific to applications such as precision e-meters and flow meters.

The TMS320C6000 DSP platform comprises the TMS-320C64x, TMS-

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CS4245/CS5345

Consumer electronic designers now have an integrated IC solution that delivers premium audio performance and streamlines product development while reducing board design complexity, size and cost.

Cirrus Logic's new CS4245 stereo CODEC and CS5345 stereo ADC are pin-compatible, highly integrated audio converters. The front-end of both IC's features an integrated analog input selector to accommodate up to 6 stereo audio sources. Also included is a programmable gain amplifier capable of ±12 dB analog gain in 0.5 dB step sizes with zero crossing, click-free transitions to maintain audio quality. One pair of inputs has a dedicated microphone pre-amplifier in its path that provides +32 dB of gain.

A multi-bit Delta-Sigma stereo A/D converter provides 24-bit conversion and output sample rates up to 192 kHz. A high-pass filter is included for DC offset removal, and a dedicated pin is available for detecting overflow conditions. The 24-bit, 192 kHz stereo DAC in the CS4245 stereo CODEC is also based on a multi-bit Delta-Sigma architecture, includes digital attenuation, and provides high-quality single-ended outputs with Cirrus Logic's patented Popguard® technology to eliminate power cycling clicks and pops.

Applications

- DVD recorders
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- Digital televisions
- Set-top boxes and home media centers
- Automotive entertainment systems
- PC sound cards
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320DM64x and TMS320C62x fixed-point generations as well as the TMS320C67x floating-point generation. The C64x generation of high-performance DSPs targets broadband and video infrastructure as well as video and imaging applications. The DM64x generation of programmable DSP-based media processors targets streaming and multimedia applications. The C62x fixed-point family targets multichannel, multifunction applications; the C67x floating-point DSP generation targets home audio, industrial automation, voice and speech recognition, as well as high-end graphics and imaging.

The TMS320C5000 DSP platform comprises the TMS320C54x and TMS320C55x fixed-point generations. The C54x generation consists of more than 17 code-compatible devices covering a range of performance and peripheral options, as well as low-power operation. The TMS320C55x generation includes power-efficient DSPs. The new TMS320C5503, TMS320C5507, and TMS320C5509A DSPs offer a combination of performance, memory, peripherals, and low power, targeting mobile, portable, and other low-power, real-time-signal-processing applications. These devices feature standby power at 0.12 mW. The new TMS320C5405, a 16-bit, fixed-point DSP available in a 7×7-mm package targets systems emphasizing small size, low power consumption, and lower cost.

Texas instruments also released the C5000 Low-Power Design Tools within the eXpressDSP tools. The design-tool suite includes power-planning tools to create trial configurations and determine the net power consumption; power-management routines within the DSP/BIOS to automatically implement power saving strategies at the operating-system level; a power-scaling library to implement power scaling through dynamic control of the runtime core frequency and voltage; and integration with National Instruments' application power-measurement tools to help designers visually measure and analyze power in their systems.

Texas Instruments' TMS320C2000 digital-signal controllers combine DSP technology with microcontroller-peripheral integration. The TMS320C28x generation includes 32-bit DSP-based controllers with onboard flash memory or ROM and offers performance to 150 MIPS for control algorithms in real time, such as sensorless speed control, random PWM, and power-factor correction supporting control-, automotive-, and industrial-motor applications. The TMS320C24x generation offers 20 to 40 MIPS of DSP performance with integrated flash memory or ROM and targets control algorithms in cost-sensitive and space-constrained applications, such as consumer white goods.

Texas Instruments and Ateme jointly announced the network-video-development kit, based on the 1-GHz TMS320C64x DSP, targeting broadcast head-end and advanced digital-media and video applications. Texas Instruments and Wintech Digital Systems offer the videophone-development platform for designing point-to-point IP-based videophone systems using the 600-MHz DSP-based TMS320DM643 digital-media processor.

You can reach Technical Editor Robert Cravotta at 1-661-296-5096, e-mail rcravotta@edn.com.

3DSP

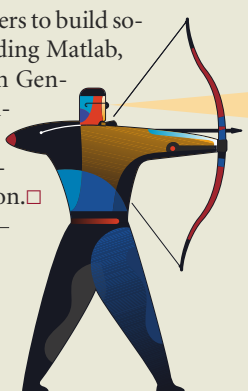
The soft-IP-core, fixed-point DSP family, bus controller, peripherals, and microprocessor interfaces from 3DSP use a scalable 32-bit SuperSIMD architecture. The core supports multiprocessor systems, program cache or direct-mapped program memory, prioritized interrupts, and a JTAG-only debugging interface. The 3DSP core supports two SIMD multiplier options. The first option is a dual 24×16-bit multiplier that can perform two 24×16-bit multiplies, four 16×16-bit multiplies, or eight 8×16-bit multiplies in a single cycle. The second option is a dual 32×32-bit multiplier that can perform all the functions of the 24×16-multiplier and two 32×32-bit multiplies in one cycle.

The programmable, five-stage-pipelined DSP SP-3 core targets MP3-player, home-audio (AAC, AC3), wireless-GSM-phone, GPS, and CPE (customer-premises-equipment) VOP (voice-over-packet)-processing applications. The programmable, superscalar, dual-issue, five-stage-pipelined SP-5 core DSP targets 3G wireless, VOIP gateway, xDSL, MPEG2, MPEG4, and wireless-LAN applications. The programmable, dual-mode, nine-stage-pipelined SP-20/UniPHY DSP-IP core targets multimedia applications including multimedia over wireless. The "soft-datapath" technology and programmability enable a "softPHY" implementation that facilitates modification for changing physical-layer standards.

XILINX

Xilinx supplies programmable-logic devices, design tools, algorithms, and services. The Virtex-4 family of FPGAs delivers as many as 512 500-MHz XtremeDSP slices that target high-performance applications, such as digital radios and baseband cards for narrowband, spread-spectrum, multicarrier communication systems, and high-performance video- and image-processing systems. The lower cost Spartan-3 family of FPGAs targets high-volume applications, such as multimedia boxes and displays.

Xilinx and its partners support Xilinx XtremeDSP, which includes more than 100 algorithms, and the System Generator for DSP tool, which enables designers to build sophisticated systems including Matlab, Simulink, and HDL models. System Generator allows designers to automatically generate FPGA bit streams and supports high-bandwidth hardware in the loop for system verification.□



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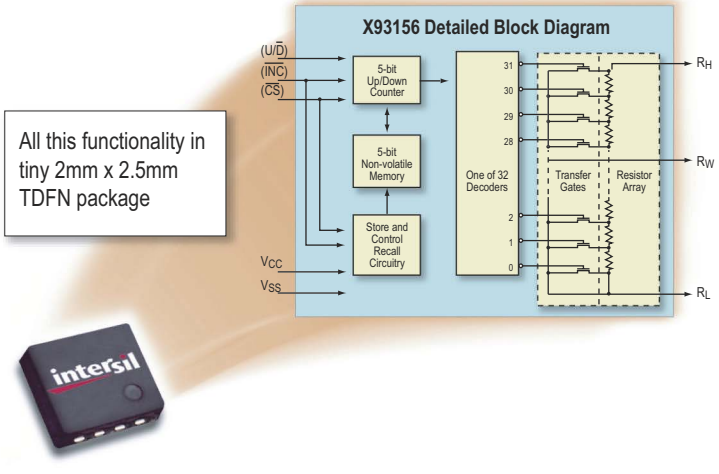

Features

- 3-wire up/down interface
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- High reliability with endurance 200,000 data changes per bit and register data retention of 100 years
- Available in 8-lead MSOP and TDFN packages
- Pb-free and RoHS compliant packaging available

Key Parameters

Description	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	X93154	2.7	3	3.3	V
	X93155	4.5	5	5.5	V
	X93156	2.7	-	5.5	V
End-to-end Resistence		35	50	65	kΩ
R_H, R_L Terminal Voltages		0	-	V_{CC}	V
Power Rating	R_{TOTAL} = 50 KΩ	-	-	1	Mw
Noise	Ref: 1kHz	-	-120	-	dBV
Wiper Resistance	X93156	-	-	1100	Ω
Wiper Current		-	-	0.6	mA
Resolution		-	3	-	%
Temperature (Industrial)		-40°C	-	+85°C	C

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By Dave Brotton, Zetex Semiconductors

DESIGNING A SWITCHING AMPLIFIER IS ONE THING; DESIGNING ONE THAT SOUNDS GREAT IS ANOTHER.

Sound advice for Class D amplifiers

Class D switching amplifiers bring undeniable benefits to audio applications in circuit efficiency, size, and cost improvements. But meeting the needs of today's consumer electronics—such as audio-video receivers that demand more than 100W of output power with less than 0.05% distortion and more than 100-dB dynamic range—can be challenging using Class D amplification. These amplifiers also have to "sound good," a requirement that's far more subjective than simply measuring and meeting target specifications for distortion noise and dynamic range. Analysis of a well-designed Class D amplifier yields a number of practical design guidelines that can help you to meet all of these goals.

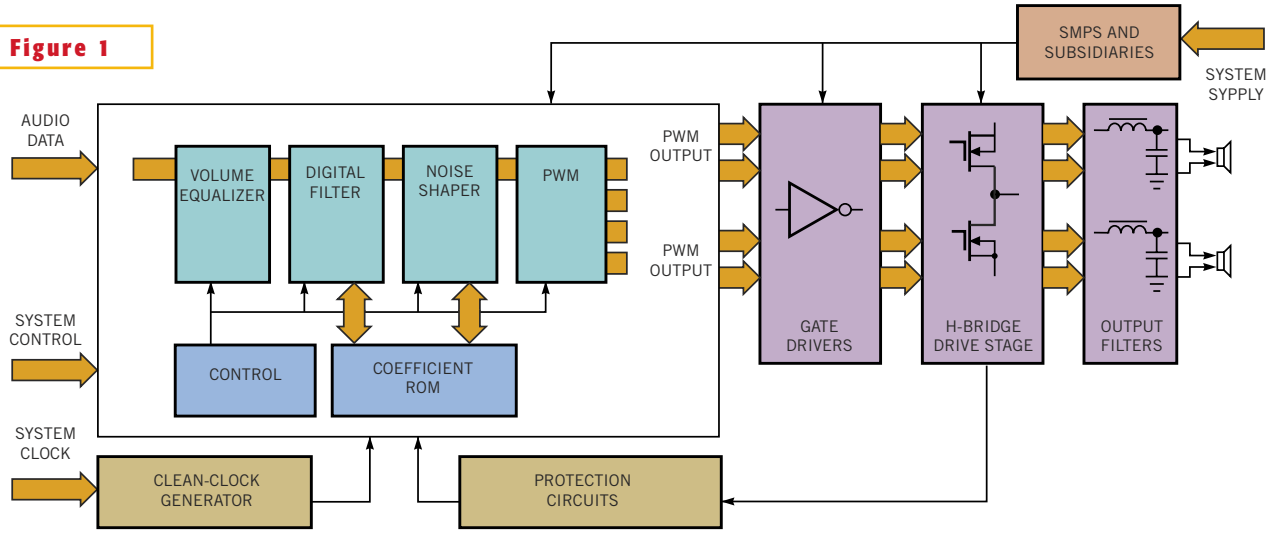
The key to a Class D amplifier's efficiency improvements over Class AB amplifiers is the use of a switching output stage rather than a conventional linear one. In a traditional analog-audio environment, a typical system requires a modulator to convert incoming signals to a PWM (pulse-width-modulation) bit stream and an output-driver stage and filter to convert the PWM back to analog power levels that suit the load. Contemporary digital-audio environments, such as CD and DVD, directly provide serial data, which can be processed in the digital domain before interfacing with the output-driver stage (**Figure 1**). This requirement leads to a new class of amplifier ICs—digital modulators—which feature controls, such as volume and equalization, and key processing circuits, such as noise shaping and digital filtering, to enable signal reconstruction.

Modulator bit-resolution, noise-shaper order, and the relationship between PWM- and master-clock frequencies all considerably influence audio quality. Another key consideration is the architecture of the on-chip digital filters, which help to maintain the detail of the recovered audio signal. The output driver also requires careful design to preserve pulse shape, minimize distortion, and ensure the best audio performance. Protection circuits are essential for safe operation, especially at high output-power levels, but they, too, must not compromise sound quality. The effects of power-supply and reference-clock quality on overall system performance are also important factors to consider.

MODULATOR

Digital filters are fundamental to the modulator architecture. Coefficients that relate to the tap length of the filter repeatedly multiply data samples. The effect of this process can degrade audio performance. Consider current audio standards, such as DVD-A, which can feature a maximum bit resolution of 24 bits; conventional digital amplifiers have internal datapaths of only 24 bits. In the multiplication process, this situation leads to the truncation of lower levels within the input signal to keep the larger signals within the available bit size. The result is a loss of low-level signal accuracy, degrading the listener's ability to hear background detail and hampering depth perception. A modulator with higher bit res-

Figure 1



A typical digital-input Class D amplifier converts audio signals to a high-power PWM filtered output before delivery to the load.

olution produces less truncation, so audio quality improves accordingly. In practice, a 32-bit modulator offers a perceptible advantage, but it's debatable whether finer resolution further improves sound quality.

FILTERING, TAP LENGTHS, AND TRANSIENTS

The FIR (finite-impulse-response) interpolation filter is a key element within any digital amplifier. Typically, these filters employ oversampling techniques to shift the aliasing images of the input signal beyond the audio spectrum. Such images exist at the harmonics of the data's sampling frequency. The implementation of the filter can introduce various compromises that you must consider when selecting a modulator to minimize their impact on audio performance.

General practice removes images at as high as eight times the sampling frequency—as high as 352.8 kHz for 44.1-kHz recordings, for example. Analog filters can remove images beyond this limit. Some modulators oversample as many as 48 times, rather than the conventional eight. This higher order filtering ensures that very-high-frequency images neither generate intermodulation distortion nor degrade the jitter performance of noise shapers.

Higher sampling rates can improve sound quality, as comparisons between DVD-A's 96-kHz recordings and CD's 44.1-kHz offerings demonstrate. However, compromises between silicon area and speed can limit the capabilities of a digital modulator's on-chip filters. An ideal filter would have a brick-wall cutoff characteristic that would require an infinite tap length, which is impractical. Generally, modulators with long taps are preferable; 256 taps represent one of today's longer implementations.

Even so, many systems with high oversampling levels and long taps include filter-performance compromises that create signal-reproduction inaccuracies. One explanation for this sound-quality degradation is the loss of transient timing information within the audio signal. Zetex, for instance, claims that its proprietary ZTA-filter algorithm preserves such timing information, which is critical to the sonic performance of its amplifiers. Successfully combining high oversampling levels with long filter tap and preserving transient information can achieve smoother, more focused sound quality, with a deep and precise sound stage and tight bass definition.

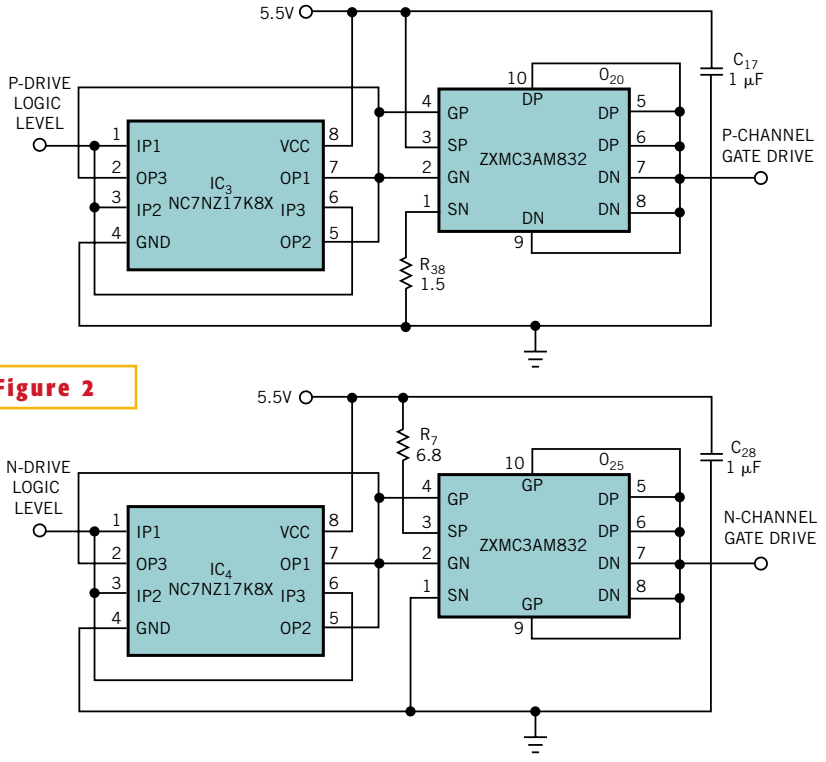


Figure 2

Tiny logic devices and complementary FETs provide high-speed drive for bridge-FET gates.

NOISE SHAPER, PWMs, AND RESOLUTION

A Class D amplifier that employs digital processing has an apparent disadvantage compared with its analog equivalent. Although digital PWM produces a quantized output signal, analog-PWM architectures offer theoretically infinite pulse-width resolution. To compensate, digital amplifiers employ noise shaping to reduce errors that the finite resolution causes. Noise shaping is conceptually an averaging process, but the process in reality is recursive. Because the PWM frequency is much higher than the highest frequency audio content, it's easy to correct errors in any given pulse width with a subsequent pulse.

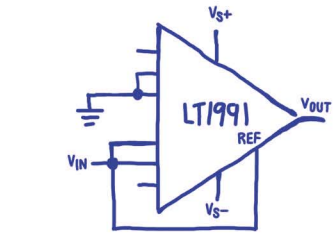
Many digital modulators employ a PWM noise-shaping system that switches at 384 kHz with a 98-MHz master clock for a 48-kHz sample rate. Other topologies can improve audio performance, such as lowering noise at higher frequencies. For example, the Zetex ZXCW-8100 uses a 1-MHz PWM switching frequency; a 33-MHz master clock; and a fourth-order noise shaper, which yields a resolution of 33-to-1, or about 5 bits. The 384-kHz system's resolution is around 255-to-1, or about 8 bits. The 384-kHz system appears to have a resolution advantage of 255/33, or around 18 dB. But if you consider the correction its noise shaper gives, the 1-MHz architecture holds the advantage. Because noise shapers correct at nominally 6 dB per order per octave, a fourth-order noise shaper corrects at around 24 dB/octave. If the two noise-shaper architectures were the same, the 1-MHz system's advantage would be 1M/0.384M, or 2.6—equivalent to 1.38 octaves.

In practice, the 1-MHz device runs its noise shaper at twice the PWM frequency by converting on both edges of the clock, so its advantage is 2.38 octaves, or 57 dB; overall, the 1-MHz noise shaper's advantage becomes 57−18 dB, or 39 dB.

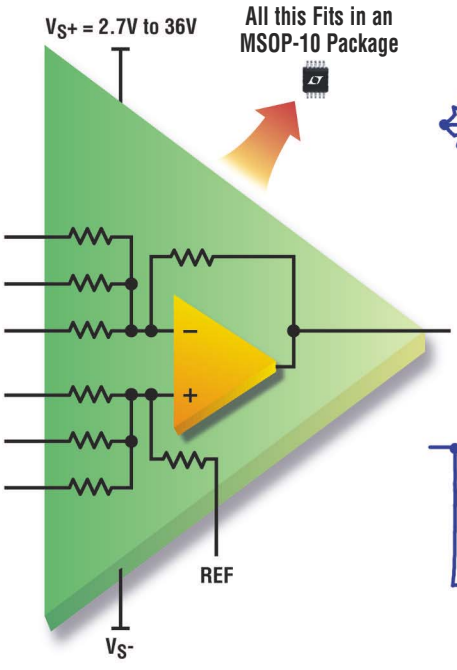
Because 384-kHz systems use higher order noise shapers, such as seventh-order, you might expect each additional order to provide another 6-dB improvement. This situation rarely occurs, however. Even if you achieve an 18-dB improvement from the 384-kHz system's three additional orders of noise shaper, the 1-MHz architecture still wins.

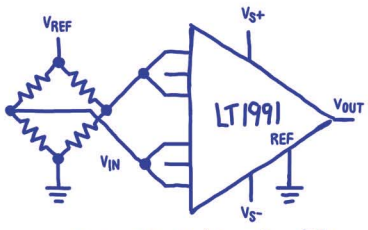
After the modulator, the PWM output requires amplification to drive a speaker, almost invariably using power MOSFETs in a bridge configuration. Gate-driver circuits must provide level-shifting

Go Configure

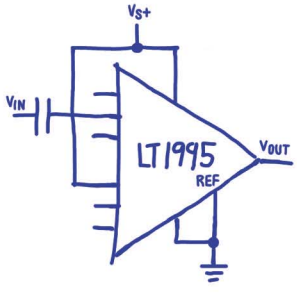


Non-Inverting Gain = 5

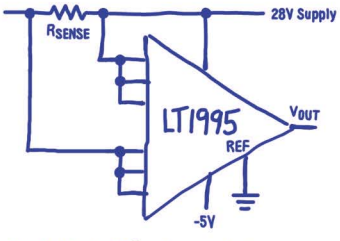




Gain of 10 Bridge Amplifier



Single Supply AC Coupled Amplifier



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	Non-Inverting	G = 0.07 to 14	G = 1 to 8
	Inverting	G = -0.08 to -13	G = -1 to -7
Specifications	Gain Accuracy (Max.)	0.04%	0.20%
	Gain Drift (Max.)	3ppm/°C	25ppm/°C
	V_{OS} (Max.)	50µV	2.5mV
	Gain Bandwidth	560kHz	30MHz
	Slew Rate	0.12V/µS	1000V/µS
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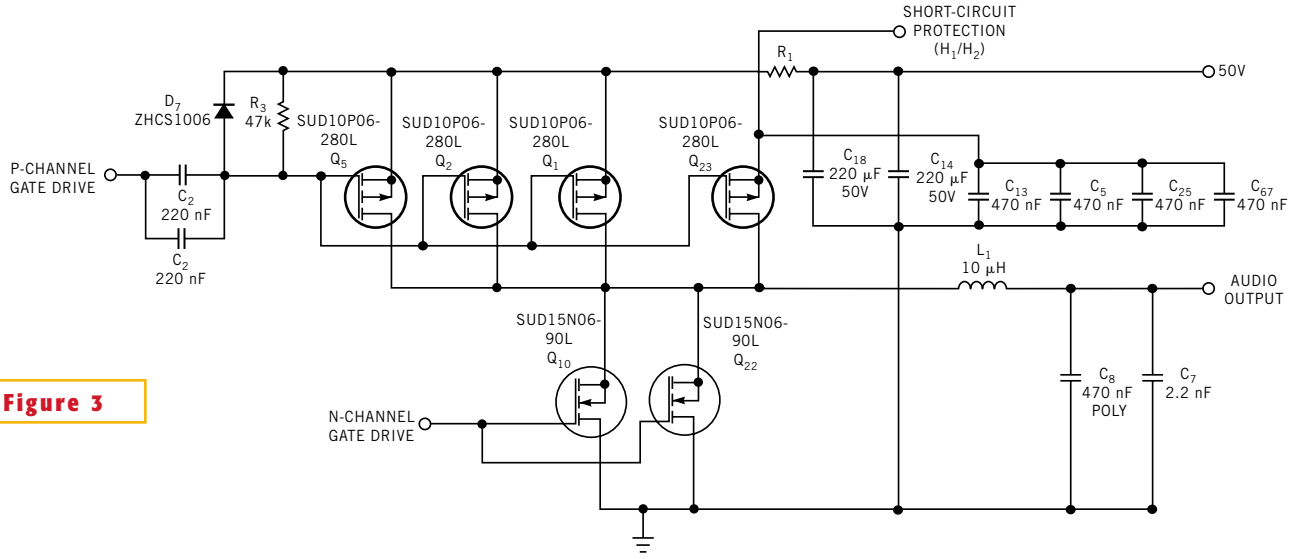
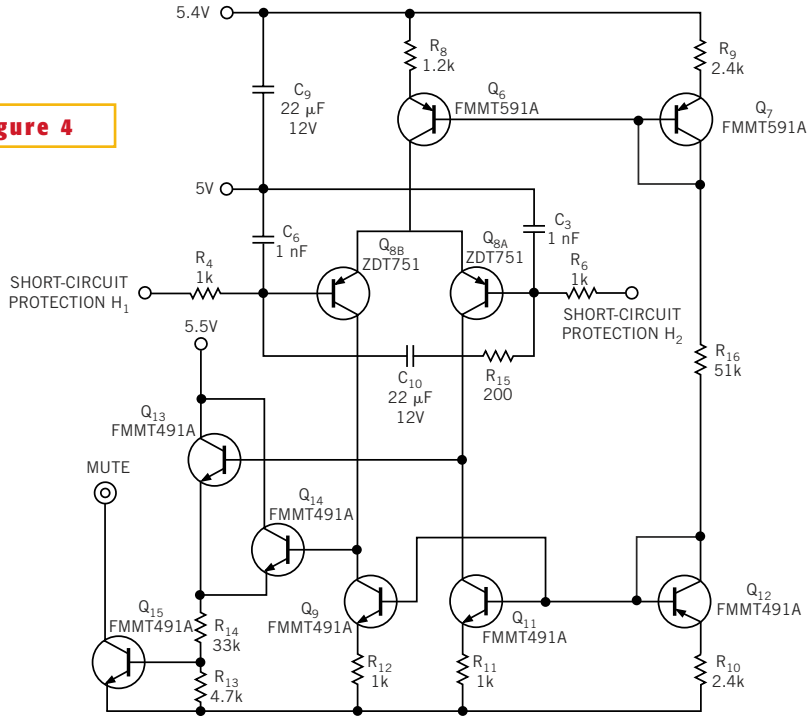


Figure 3

Complementary FETs in a BTL configuration show one-half of the BTL output bridge.

and current drive but without distorting pulse shape (**Figure 2**). These circuits use tiny NC7NZ17 logic devices with complementary ZXMC3AM832 FETs to provide a high-current, high-speed drive to a bridge in a 1-MHz PWM system. Speed is critical to maintaining the pulse integrity that preserves dynamic range and minimizes distortion. A 33-MHz master clock and 1-MHz PWM clock require a 30-nsec pulse resolution; typically, the driver must switch in 8 nsec and support about 4A peak current. Because a significant trade-off exists between distortion and dissipation in the bridge, it's also essential to control the shoot-through current that flows in the fractional time that both top and bottom bridge FETs conduct. Here, resistors in the gate-drive buffers limit shoot-through by controlling the on-times of the N- and P-channel FETs. P-channel control focuses more on minimizing ringing, but slowing the N channel's on-time balances its switching point to match the slower P channel's response.

Figure 4



This bridge-sense circuit protects an amplifier that can deliver 150W into 8Ω.

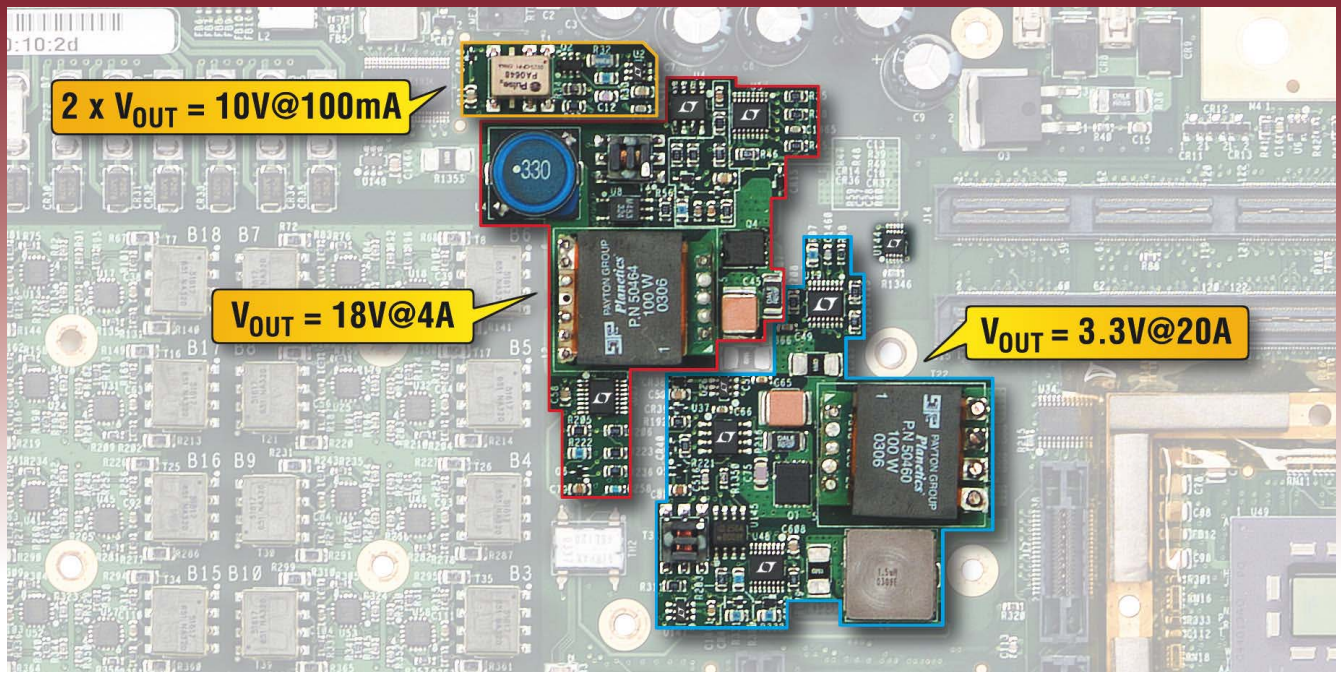
OUTPUT-STAGE BRIDGE DESIGN

Because Class D amplifiers typically use an open-loop topology, there's no benefit from feedback. Audio performance can then be susceptible to matching errors in the bridge. A single-ended output is simple and offers the possibility of bridging outputs to deliver more power but lacks inherent cancellation. A full H-bridge optimizes cancellation to provide the best performance and delivers maximum power from any given supply voltage.

In designing a bridge, you can choose complementary or all-N-channel devices. Complementary bridges are simpler to drive, because all-N-channel versions require bootstrap circuits to enhance the high-side FETs. Power levels below about 200W into 8Ω favor complementary bridges, but finding appropriate P-channel devices becomes increasingly difficult above this level. **Figure 3** shows one-half of the bridge using complementary FETs in a full BTL (bridge-tied-load) configuration.

The output bridge uses 60V-rated Vishay-Siliconix SUD10P06-280L and SUD15N06-90L devices that can switch 15A in about 20 nsec. Parallel operation of FETs is a good choice for several reasons. First, current sharing minimizes dissipation and allows good thermal design with minimum heat-sinking. Parallel operation also enables the FETs to operate on the most linear part of their on-resistance versus current curve. This

48V to Any Volts



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Function	Part Number	Description	Package
Flyback Controllers	LTC®3803	Constant Frequency 200kHz with adjustable slope-compensation	ThinSOT™
	LT®1725	No optoisolator required; Senses V_{OUT} from primary side winding	SO-16, SSOP-16
	LT1737	No optoisolator required; Low 4.5V_{MIN} supply voltage	SO-16, SSOP-16
Single Switch Forward Controllers	LT1952	Synchronous; Programmable volt-second clamp	SSOP-16
	LT1950	3V to 25V input voltage range; Onboard auxiliary boost converter	SSOP-16
	LTC3900	Secondary side synchronous rectifier driver for forward controllers	SO-8
2-Switch Forward Controllers	LTC3705	PolyPhase™; No need for separate bias regulator	SSOP-16
	LT3781	72V operation; Synchronizable for multiple controller systems	SSOP-20
Push-Pull Half- & Full-Bridge PWM Controllers	LTC3723	Synchronous; Adjustable dead-time and synchronous timing	SSOP-16
	LTC3721-1	Adjustable dead-time; 4mm x 4mm QFN package	SSOP-16, QFN
	LTC3901	Secondary side synchronous driver for push-pull and full-bridge	SSOP-16
Full-Bridge ZVS Controller	LTC3722	Current and voltage mode with adaptive or manual delay control for zero voltage switching	SSOP-24
Secondary Side 2-Switch Forward Controllers	LTC3706	Fast, PolyPhase current mode	SSOP-24
	LTC1698	Secondary side synchronous rectifier controller	SO-16
Secondary Side Post Controllers	LT3710	Regulated auxiliary output in isolated DC/DC converters; Synchronous drivers; Programmable current limit	TSSOP-16
	LT3804	Regulates two secondary outputs; Integrated optocoupler driver	TSSOP-28
MOSFET Drivers	LTC4440	80V operation; 100V transient tolerant; Fast gate drive	ThinSOT, MSOP-8
	LTC4441	6A peak output current; 5V to 8V adjustable gate drive	MSOP-10; SO-8
	LTC1693	Single & dual N-, P-channel MOSFET drivers	SO-8, MSOP-8
Optocoupler Driver	LT4430	600mV, 1% accurate reference; prevents overshoot	ThinSOT
Overvoltage Protection Controller	LTC1696	±2% overvoltage threshold accuracy; Gate drive for SCR crowbar or N-channel disconnect MOSFET; Monitors two output voltages	ThinSOT

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detail is important, because any on-resistance modulation can cause odd-order harmonic distortion. In this example, parallel devices reduce output impedance, resulting in an increase in damping factor, improving the tightness of the bass response. Here, the output impedance is 0.2Ω—equivalent to a damping factor of 40 with an 8Ω load.

A lowpass filter removes high-frequency content before the speaker. Typically, these filters require a frequency response that's flat up to 20 kHz, but some audio standards demand a controlled response up to 96 kHz. For good audio performance, the inductors provide excellent linearity characteristics and a tolerance of only a few percentage points. They also require minimal series resistance and core losses and must not saturate under heavy load conditions. Distributed-air-gap, iron-powder cores are often the best choices.

The system's PWM frequency affects output component values, and the 1-MHz architecture minimizes inductor size. This high-frequency switching also enables a higher filter-cutoff frequency, which helps meet specifications such as SACD (super-audio compact disc) with a high degree of tolerance to variable-impedance loads. Filter capacitors are similarly critical, because poor-quality components can increase THD (total harmonic distortion) and degrade reliability. Use RF-quality, low-ESR (equivalent-series-resistance) types.

Adequately protecting an amplifier is not trivial. Any scheme must operate correctly with widely varying dynamic conditions, both in signal level and output-load impedance, but must trip if a fault occurs, regardless of audio conditions. Ensuring protection with shorts at the smallest signal levels can be more important than the more obvious high-power conditions.

First, consider whether you're protecting the amplifier, the load, or both. Then, consider the fault conditions that you need to guard against. Conventional protection ensures that users can abuse the external connections of an amplifier without damaging it or the speaker. However you apply it, the protection circuit must trip whenever a short across the amplifier outputs or a short from any amplifier output to ground occurs.

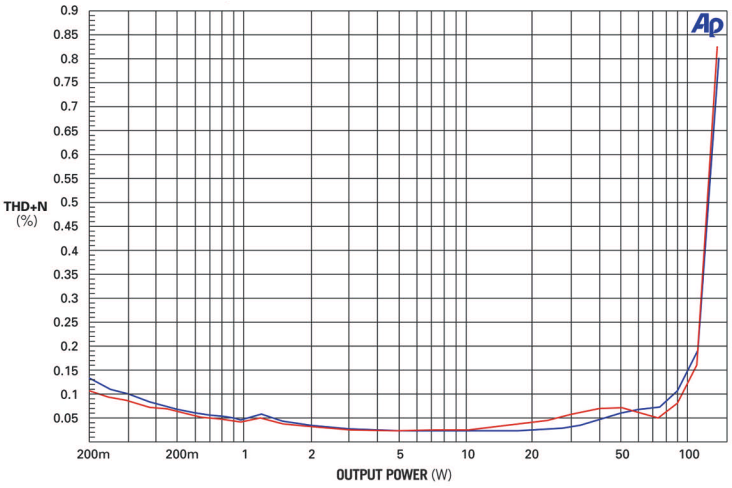

Figure 5 A 10-mΩ sense resistor in the bridge power rail causes minimal additional distortion.

SHORT-CIRCUIT PROTECTION

Current-sense circuits normally provide short-circuit protection, either within the system's power supply or directly at the bridge; a combination of both can offer excellent protection. Current limits in the power supply are easy to apply, because they're often parts of the standard SMPS (switch-mode-power-supply) circuit; applying protection in the bridge is somewhat more difficult. **Figure 4** shows a bridge-sense circuit that protects an amplifier that can deliver. 150W into 8Ω. **Figure 3** shows the sense components. Sense resistors between the positive bridge supply and each half of the output bridge (10-mΩ R_1 in **Figure 3**) develop voltages proportional to the current flowing in the bridge. These voltages supply the differential inputs of the protection circuit—in this case, a ZDT751 dual-PNP transistor (Q_8). When an overcurrent of sufficient magnitude occurs, the differential voltage drives "mute" low.

Circuit setup is important. For example, the balance between C_{10} and R_{15} desensitizes the inputs to fast transients. Output-filter-inductor choice is critical, too, because circuit operation relies on nonsaturating inductors. Select components with a saturation current well above the expected amplifier's maximum output current under normal conditions. In this example, inductors with saturation current well over 20A suit a trip point of 12A. Also consider speaker impedance variations. In this case, allowing for a 4Ω load requires a balance between trip-point selection and the current that's necessary for full power into 4Ω. This circuit setup cuts in somewhat below 3W, a level low enough to allow safe operation of the amplifier driving into shorts with the lowest of signal levels.

Power supplies have a profound influence on audio performance. As a result, a sense resistor in the bridge supply rail can influence audio quality. In practice, measurements confirm that the 10-mΩ sense resistor causes minimal degradation (**Figure 5**).

Open-loop Class D amplifiers demand extra consideration for the influence of support circuits. The system's power supply, particularly the supply to the bridge, is a major contributor (see **sidebar** "Power-supply quality and capacity for details" with the version of this article at www.edn.com). Poor system clocks may also degrade sound quality (see **sidebar** "Keep system clocks clean," also with the Web version of this article).

The study of many implementations of digital-input Class D circuits shows how easy it is to create an amplifier that doesn't do itself justice in measurement or sound quality. Although time and space do not permit this article to consider every angle of design, practical implementation and attention to the key areas can significantly enhance performance and potentially produce the best sounding digital amplifiers.□

Author's biography

Dave Brotton is a technical marketing manager for audio products with Zetex plc, where he has worked for 13 years, originally as product-line manager for power-management products and for the last four years developing the Zetex Class D switching-audio program.

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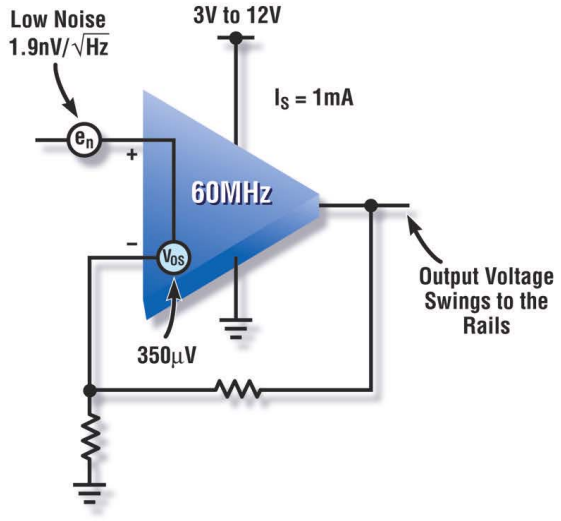

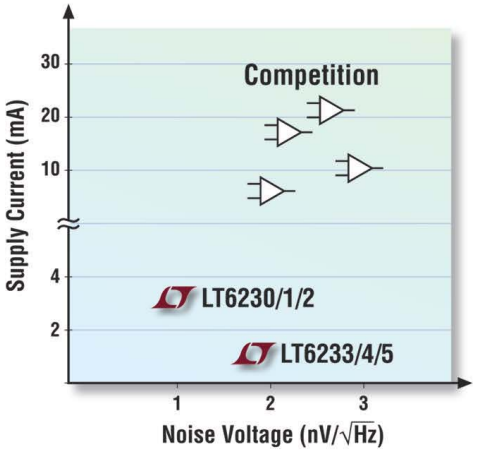

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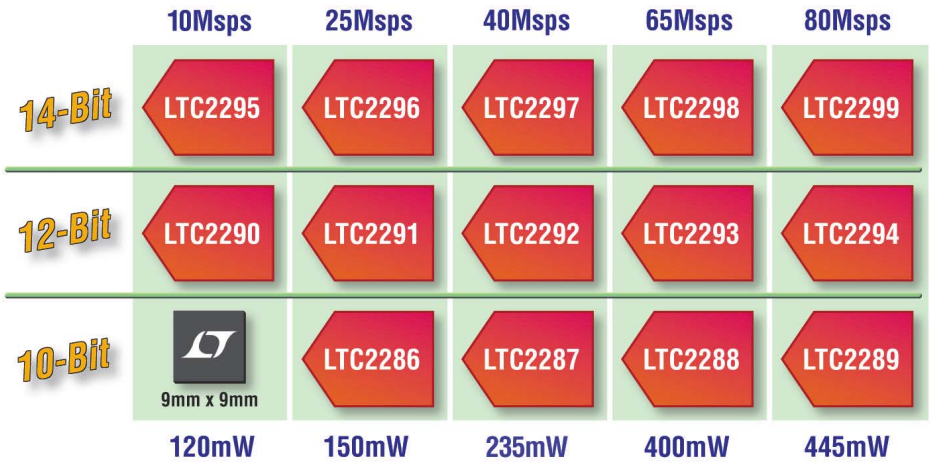

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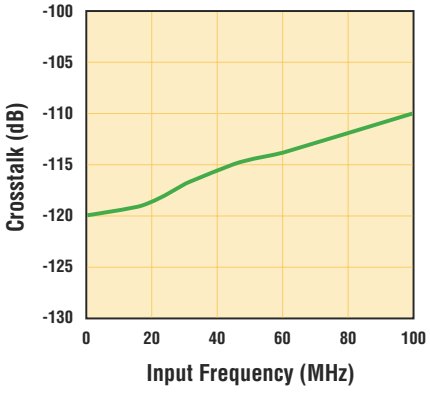
Crosstalk vs Input Frequency



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DESIGN NOTES

Simple Battery Circuit Extends Power over Ethernet (PoE) Peak Current – Design Note 361

Mark Gurries

Introduction

Power over Ethernet (PoE) is a new development that allows for the delivery of power to Ethernet-based devices via standard Ethernet CAT5 cable, precluding the need for wall adapters or other external power sources. The PoE specification defines a hardware detection protocol where Power Sourcing Equipment (PSE) is able to identify PoE Powered Devices (PDs), thus allowing full backwards compatibility with non-PoE-aware (legacy) Ethernet devices. The PoE specification also sets an upper limit on the power that can be drawn by a PD. The problem is: what happens when a PD must draw more power than allowed by the PoE standard? Examples may be the spin up of a disk drive or a period of sustained transmission of data from an RF transmitter. If the *average* power load of these

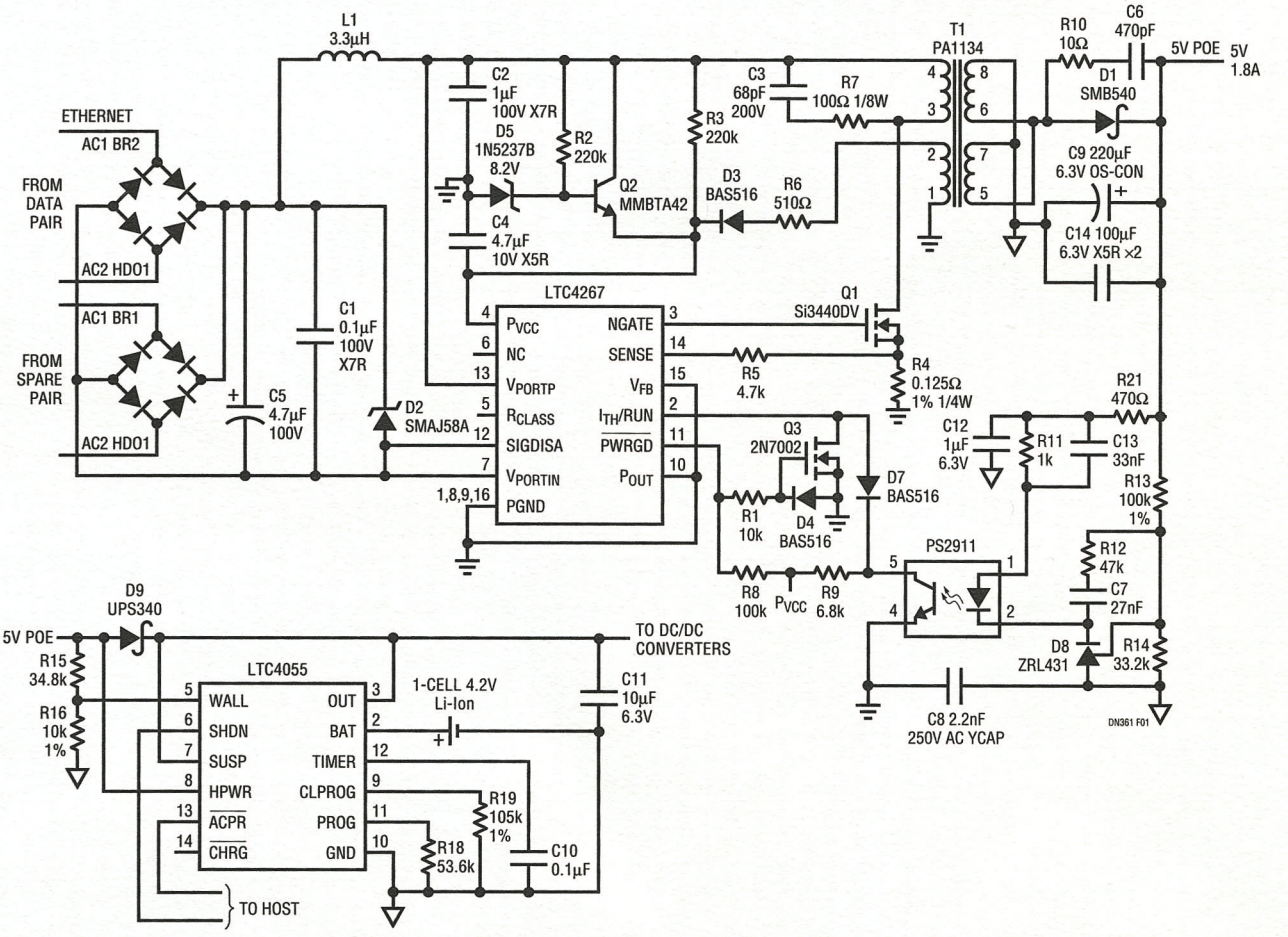

Figure 1. Simple Battery Charger/PowerPath™ Controller (LTC4055) Augments PoE Regulator's (LTC4267) Peak Output Power to Overcome PoE Power Constraints

applications is less than the available PoE power, one solution is to store power in the PD when power consumption is low and then tap the reserve to augment PoE power when needed. For many applications, a rechargeable battery fits the bill.

Of course, one can't just throw a battery and a battery charger into the mix. The power path must be able to change seamlessly, on the fly, from PoE-powers-device-and-charges-battery, to PoE-and-battery-power-device, to battery-powers-device. Figure 1 shows a complete and compact solution.

The PoE Circuit

By default, power over the Ethernet is *not* available. The standard calls for a protocol to be implemented that allows the Ethernet hub to identify the device needing power. The LTC®4267 simplifies the design of PDs by providing wholesale implementation of the protocol and power management functions.

PoE power comes in the form of –48V at 350mA. If the PoE current is allowed to exceed 400mA, the standard calls for the PSE to break the circuit. This is a problem for devices that occasionally need a little more juice than PoE will offer. Another problem is that –48V does not easily convert to commonly used positive voltage supply rails. Designers are forced to provide DC isolation along with the inverted down conversion to a more usable voltage. To meet these requirements, the LTC4267 used in Figure 1's circuit implements an input current limited DC input isolated flyback converter, providing a user-settable regulated low voltage.

The LTC4267 circuit in Figure 1 supplies 5V at 1.8A. 5V is a popular supply voltage to run logic, interface with other devices such as USB, and of primary concern in this application, to charge a single Li-Ion cell to its target termination voltage of 4.2V.

PowerPath and Charger Circuit

In Figure 1, the LTC4055 provides triple PowerPath control and Li-Ion battery charging. One path is created by connecting an external Schottky diode to the LTC4055's OUT pin and the built-in wall adapter detection circuits. In this case, the "wall adapter" power comes from the LTC4267 5V power supply called 5V PoE. The second path is for USB power, not used in this application. The third path is the battery discharge path. When the 5V PoE power goes away or drops out of regulation, the LTC4055 automatically switches the battery power over to the OUT pin using its internal ideal diode circuit. There is no delay in the switchover, so power is never lost.

When 5V PoE power is restored, the battery is disconnected from the load and charging is permitted. The LTC4055 charge current is adjustable and in Figure 1, the circuit is limited to 900mA which is drawn from the OUT pin. That leaves 900mA to run the system while charging. Powered devices connected to the OUT pin must be compatible with the Li-Ion voltage range. The $\overline{\text{ACPR}}$ pin of the LTC4055 can be used to indicate which power source is providing power, allowing the PD to configure itself accordingly.

High Transient Load or Continuous Current Load Operation

When the power limit of the 5V PoE supply is reached, the voltage drops and the battery charger shuts down to relieve the PSE of the charge current load. If the voltage continues to collapse, the battery automatically is placed into parallel operation with the 5V PoE power supply, thus increasing the available peak load current. The LTC4055 $\overline{\text{ACPR}}$ signal is active high during the overload. Battery charging automatically resumes once the overload goes away and the 5V PoE voltage has risen enough to show recovery.

Optimization Options

If sustained currents approaching 1.8A are expected from the 5V PoE and there are thermal management issues related to the diode's heat dissipation, the diode D9 can be replaced with the LTC4411 ideal diode for more efficient operation. Recommended DC/DC converters to generate logic supplies in this application include the LTC3443 buck-boost and/or the LTC3407-2 dual buck regulators.

Conclusion

The highly integrated LTC4267 and LTC4055 simplify the design of compact, simple and complete battery-based power systems that run from Ethernet power. More importantly, seamless PowerPath control enables circuits that can use a battery to augment Ethernet power when an application momentarily demands more than the PoE standard allows.

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Edited by Brad Thompson

Camera serializer/deserializer chip set reduces wire count for keypad

Wallace Ly, National Semiconductor Corp

Many systems that require a user to manually enter data feature a keyboard similar to that in **Figure 1**. Although early keypads comprised arrays of individually wired switches, a typical modern keypad comprises a matrix of x and y lines. Pressing a key creates a momentary connection between an x line and a y line. For example, an individually wired keypad comprising discrete switches arranged in four rows and three columns (also known as a 4×3 layout) would require 24 wires. The more economical matrix approach in **Figure 2** requires only seven signal wires, but even that number can sometimes prove difficult to route to a microcontroller. To further reduce the number of interconnecting wires from seven to three, plus a ground return, you can adapt a configurable serializer/deserializer such as National Semiconductor's LM2501.

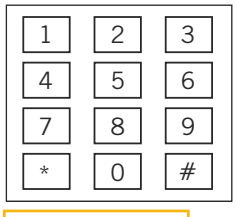

Figure 1

A typical keypad provides a limited number of numeric keys and two symbols–the asterisk (*) and the octothorpe (#).

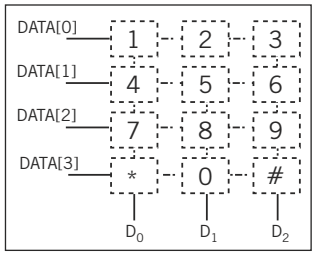

Figure 2

In a matrix keypad, pressing a key creates a connection between a row wire and a column wire.

The device typically finds use in adapting video buses, such as wide, low-voltage CMOS-video interfaces for portable electronics to Mobile Pixel Link service. The LM2501's typical application circuit features low-voltage and low-current operation and produces low levels of EMI (**Figure 3**). The circuit requires only two support devices—a counter (a CMOS CD4017 decade counter) and a 10-MHz clock-oscillator module (**Figure 4**). In operation, the host microcontroller drives the deserializer's WCLK input pin with a low-voltage-CMOS clock pulse,

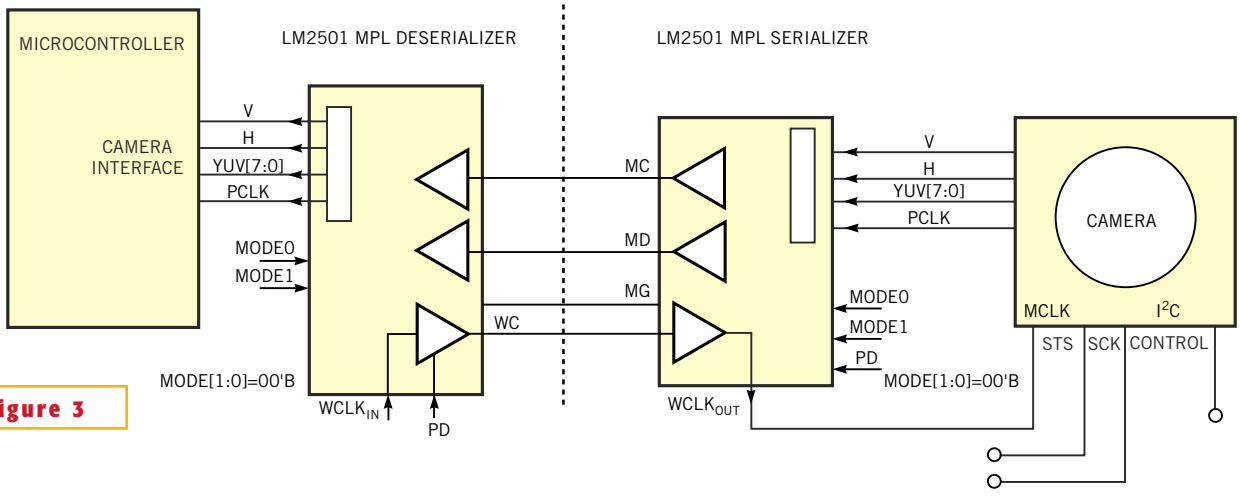

Figure 3

In a typical application, a pair of LM2501s converts multiconductor video data to serial data and restores the data to multiconductor format.

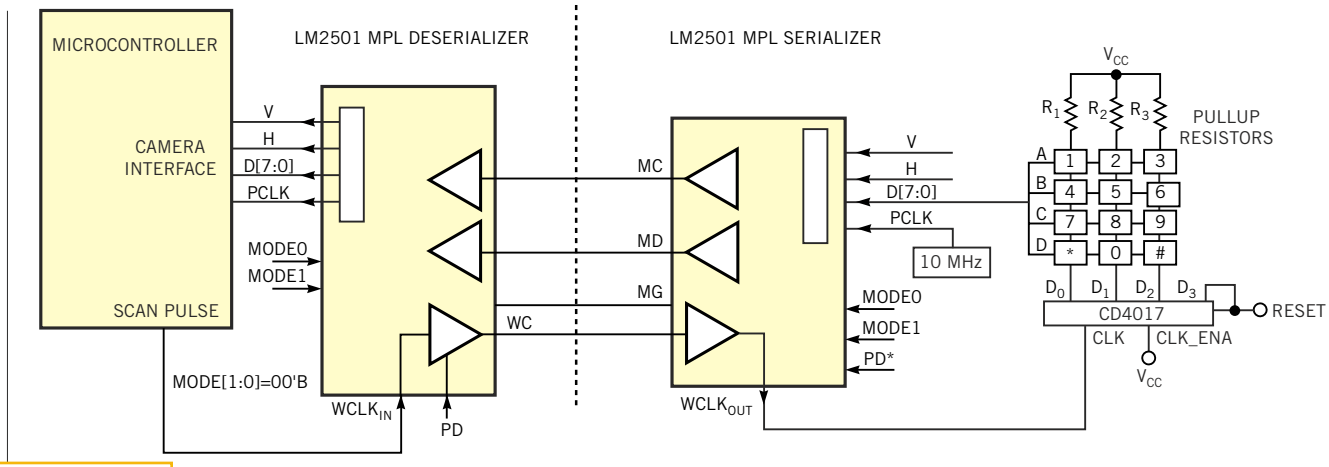

Figure 4 You can apply the LM2501 to reduce the number of signal lines a keypad-to-microprocessor interface requires.

which translates to an MPL-level signal and then is applied to the serializer. The serializer reconverts the WCLK pulse, which drives the counter's clock input.

Unlike divide-by-10 encoded-output decade counters, the CD4017's internal organization comprises a Johnson counter that activates only one of its 10 outputs at a time. Thus, the counter's outputs D_0, D_1, and D_2 sequentially apply a logic one to the keypad's column lines, and output D_3 resets the counter to zero. When a user presses a key and connects a column line to one of four row lines, the serializer samples the keypad's row lines, converts the selected active line to a serial signal, and transmits the signal to the deserializer.

For example, suppose that the user presses the 5 key. The first clock pulse that the CD4017 receives drives column line D_0 to a logic one, but, because the user does not press keys 1, 4, 7 and *, row lines A, B, C, and D remain at logic zero. The second clock pulse drives column line D_1 to a logic one, and pressing key 5 connects row line B to logic one, whereas lines A, C, and D remain at logic zero. The pseudocode fragment in **Listing 1**, available in the online version of this Design Idea at www.edn.com, instructs the microcontroller to decode which key a user is currently pressing. In practice, additional code enables the microcontroller to reject multiple simultaneous key closures.

You can expand the architecture to accommodate a keypad matrix as large as 8×10 keys by using more of the counter's outputs and wiring the Nth output to the counter's reset input. The keypad's rows connect to the serializer's data inputs, and both of the LM2501s' unused inputs connect to pullup resistors, ground, or V_{CC}.□

Rearranged reference helps ADC measure its own supply voltage

Björn Starmark and Orville Buenaventura, Maxim Integrated Products Inc, Sunnyvale, CA, and Sören Käck, Audioväxlar, Sweden

If you use an ADC to monitor a system's power-supply voltage, you may encounter situations in which the supply voltage exceeds the ADC's reference voltage (**Figure 1**). However, the ADC's input voltage cannot exceed its reference voltage. You can use an external resistive divider to bring the supply voltage within the ADC's input range, but even 0.1%-

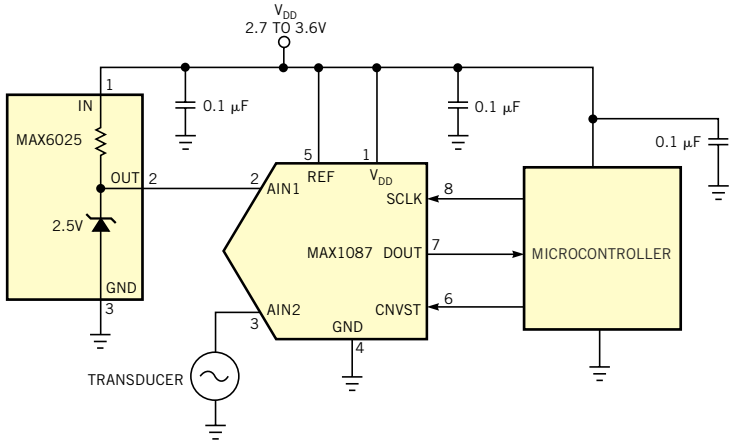

Figure 1 A precision resistive divider brings the power-supply voltage within this ADC's input range but introduces measurement errors.

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tolerance resistors may introduce an objectionable error. You can solve the problem by eliminating the divider, connecting the ADC's reference input to its power supply, and connecting one of the ADC's inputs to a precision voltage reference—in this case, a 2.5V MAX6025A (**Figure 2**).

In this configuration, the ADC measures its inputs with respect to the supply voltage. Using the digitized reference voltage as a standard, the system's software computes the ratio of the reference voltage with respect to the power-supply voltage and corrects the remaining inputs' measurements. The ADC must accommodate an external reference voltage that equals its power-supply voltage, and any noise on the supply rail disturbs measurements of all channels. Thus, to quiet the supply rail in electrically noisy environments, you may need to add a lowpass filter to provide extra decoupling at the ADC.□

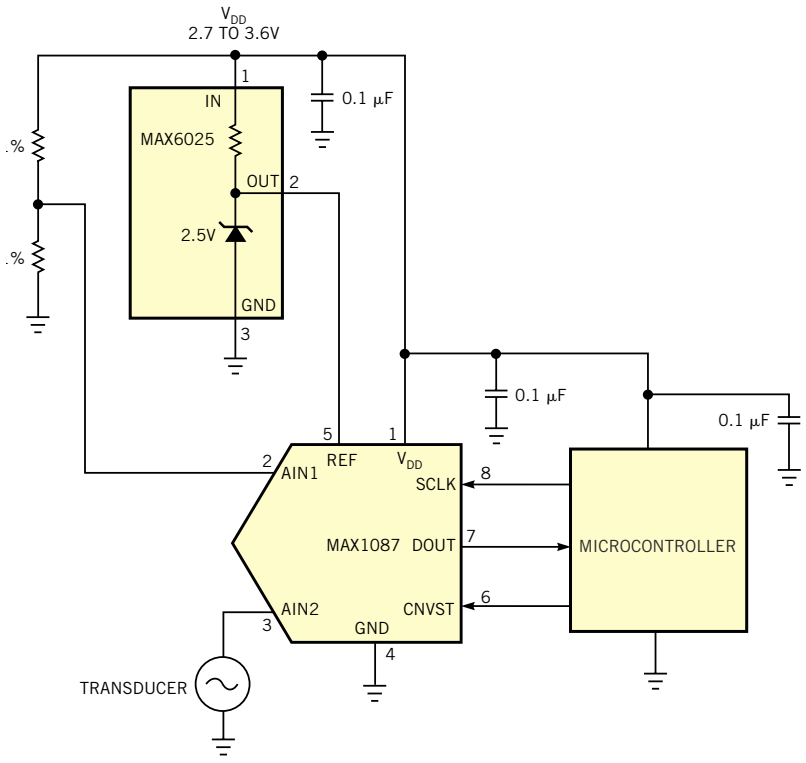

Figure 2 To eliminate the resistive divider, you connect the ADC's reference voltage to its power supply and measure the precision voltage reference's output.

Difference amplifier measures high voltages

Moshe Gerstanhaber and Chau Tran, Analog Devices, Wilmington, MA

FIGURE 1 shows two large-signal-measurement methods. The first uses a two-resistor voltage divider and an output buffer, and the second comprises an attenuating inverter and a high-value input resistor. Both of these approaches introduce measurement-linearity errors because only a single resistor dissipates power, which leads to self-heating and its associated change in resistance. In addition, the amplifier and the remaining resistors introduce a combination of offset current, offset voltage, CMRR (common-mode-rejection-ratio) effects, gain error, and drift, which may significantly reduce the system's overall performance.

Based on Analog Devices' AD629, the circuit in **Figure 2** can measure inputs in excess of 400V p-p with less than 5-ppm linearity error. The circuit attenuates its input signal by a factor of 20 and delivers a buffered output. Packaging the amplifier and attenuator resistors together ensures that both resistors in the attenuator string operate at the same temperature. The amplifier's input stage employs superbeta transistors to minimize offset current and errors due to bias current errors. Applying 100% feedback at low frequencies introduces no noise gain, and the offset voltage and its drift add almost no error.

The AD629 is unstable with 100% feedback, and the 30-pF capacitor adds a pole and a zero to the feedback gain to stabilize the circuit and maximize the

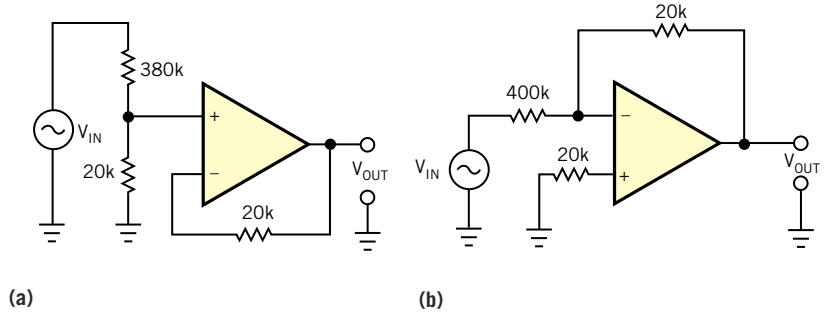

Figure 1 To measure high voltages, you can use discrete resistors to assemble an input voltage divider and buffer (a) or an attenuating inverter (b), but performance suffers due to thermal mismatch.

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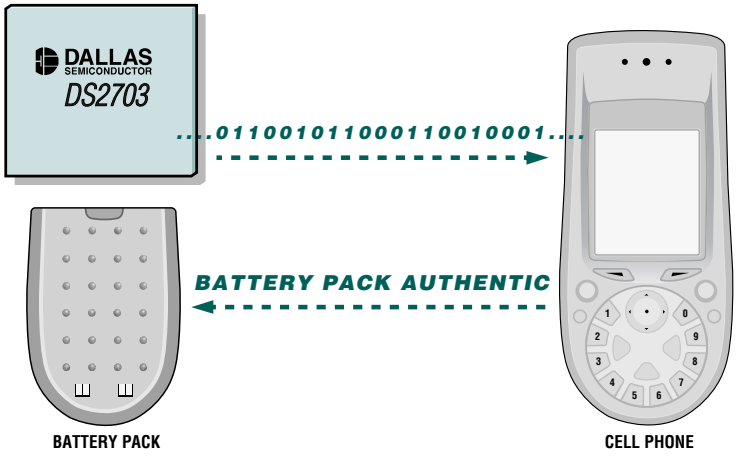

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system bandwidth. The following equation calculates the pole frequency, f_P: $f_P = 1/(2\pi(380\ k\Omega + 20\ k\Omega) \times 30\ pF) = 13$ kHz. The following equation determines the zero frequency, f_Z: $f_Z = 1/(2\pi(20\ k\Omega) \times 30\ pF) = 265$ kHz.

Figure 3 shows the amplifier's performance with a 400V p-p input (upper trace) and its corresponding 20V output (lower trace). In **Figure 4**, a cross plot shows linearity for a 50V/division input signal and a 5V/division output. **Figure 5**, a linearity-error plot, shows nonlinearity versus a 400V p-p input signal.□

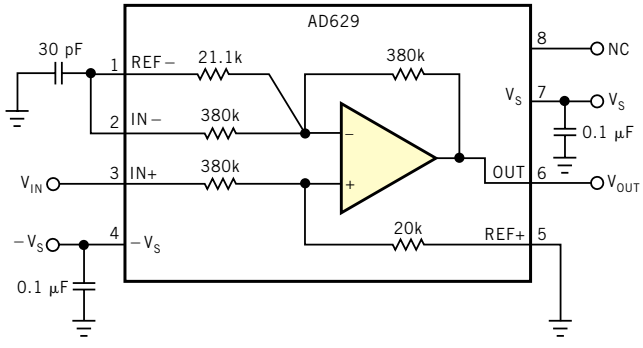

Figure 2 An integrated approach moves external resistors into the device's package for improved thermal tracking and greater accuracy.

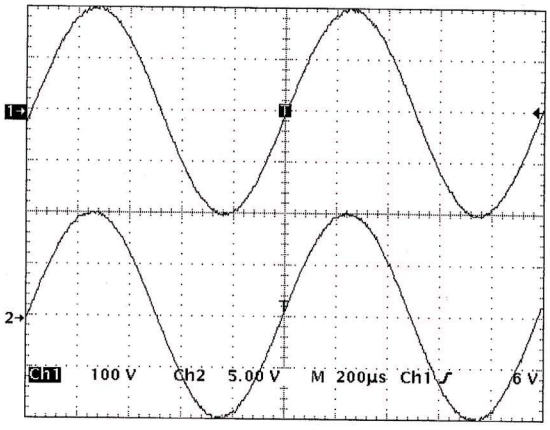

Figure 3 The circuit in Figure 2 delivers a 20V p-p output for a 400V p-p input.

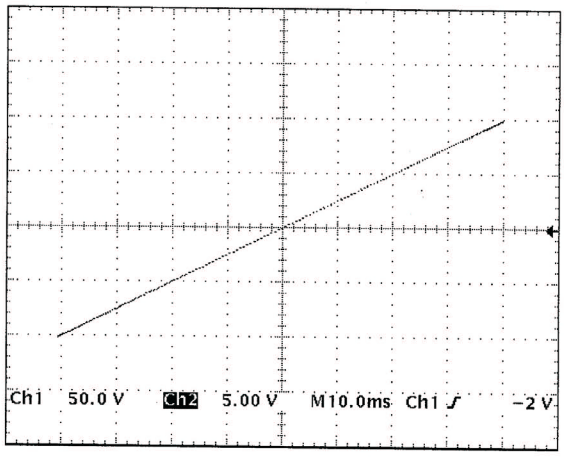

Figure 4 Plotting input versus output shows minimal departure from an ideal straight line for a 400V p-p input.

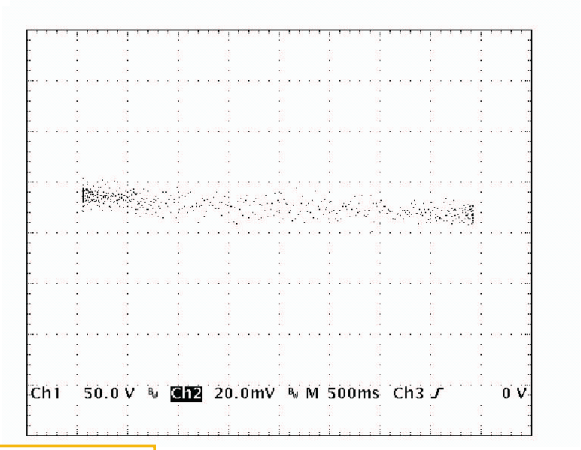

Figure 5 A scatter plot of nonlinearity error for a 400V p-p input displays error of less than 10 ppm over the input range.

Linear potentiometer provides nonlinear light-intensity control

Stephan Goldstein, Analog Devices, Wilmington, MA

THE HUMAN EYE'S highly nonlinear response to light levels poses problems for designers of adjustable lighting. Simple hardware or software linear-control methods compress most of the apparent intensity variation into a relatively small portion of the adjustment range. A strongly nonlinear control characteristic is necessary. Such a characteristic

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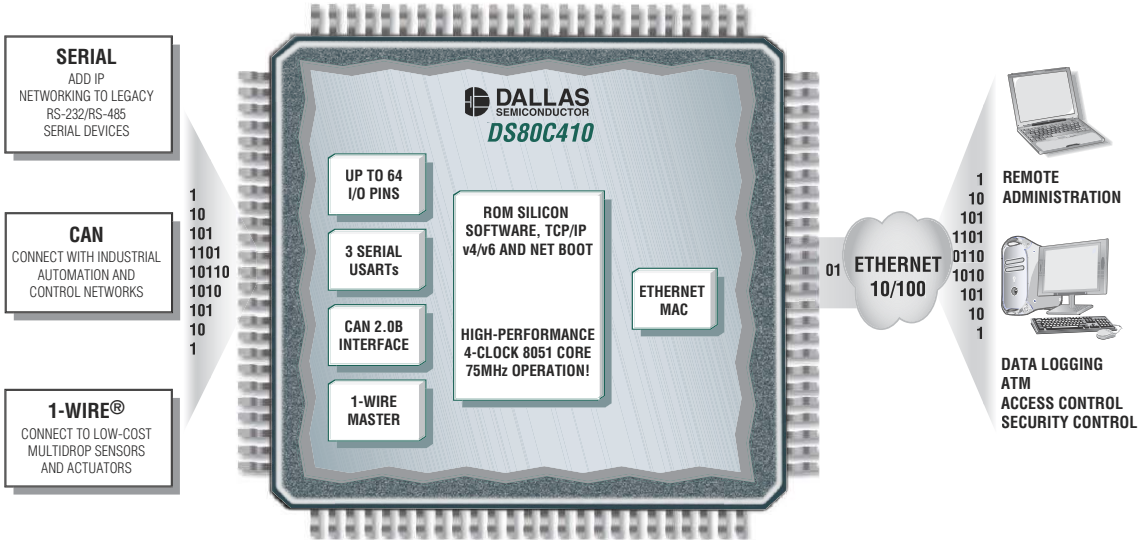

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DS80C410-FNY	73.25	1	100-LQFP	7.81
DS80C411-FNY	73.25	0		7.05
DS80C400-FNY	9.25	1		7.78

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Java is a trademark of Sun Microsystems, Inc.
SPI is a trademark of Motorola, Inc.
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spreads the intensity adjustment over a wider range and offers a more natural feel. This Design Idea shows how to use an inexpensive linear potentiometer to develop a satisfactory hardware technique. In an experiment in a darkroom, one of the room's corners was too dark because a fixed barrier shielded safe light. Using spare parts from a junk box, you could assemble a simple red LED-based auxiliary safe light, but if the light level were adjustable, you could balance the light levels and minimize the risk of fogging the printing paper. However, the experimenters in this case lacked an audio-taper intensity-control potentiometer and wanted to avoid paying for one.

Figure 1 shows a simplified version of the technique. Diode-connected transistor Q_1 and an AD589 1.235V reference, IC_1, produce a reference voltage of $1.235V+V_{BE}(Q_1)$ at Node A. Connected between Node A and Q_2's emitter, linear potentiometer R_2 and resistor R_3 cause Q_2's emitter and collector current to vary as $1.235V/(R_2+R_3)$. The relationship isn't exact because the V_{BE} voltages of Q_1 and Q_2 vary slightly as you adjust the potentiometer, but, in practice, this nonlinear—if not logarithmic—characteristic works well.

Transistor Q_2's collector current generates the control voltage across R_4, and, whereas Q_2 always operates close to saturation, the components limit Q_2's collector-base forward bias to an acceptable 200 mV. When you set R_2 to its minimum resistance for maximum light intensity, resistor R_3 limits LED current, and, when you set R_2 to its maximum resistance for minimum intensity, R_1 limits the current through IC_1.

The reference voltage produced at Q_2's collector drives a standard integrating servoamplifier comprising an AD8031 rail-to-rail op amp, IC_2; an IRFD010 low-power MOSFET, Q_3; R_5 ;R_6; and C_2. The servo sets the current through R_5 to R_4/R_5 times the current through R_4. Resistor R_7 isolates Q_3's gate capacitance to prevent load-induced instability in IC_2. A 12V-dc module supplies power to the circuit and allows the use of four LEDs per string, for a total voltage drop of approximately 8V across each string. To prevent current hogging and provide a maximum of approximately 20 mA for each series-connected LED string, resistors R_8 through R_{11} divide Q_3's drain current into four. Voltage drop across each resistor is 1V, leaving Q_3 to support a 3V drain-source voltage and an approximately 250-mW power dissipation. If you increase the number of LEDs or the power-supply voltage, you may need to replace Q_3 with a higher dissipation MOSFET.□

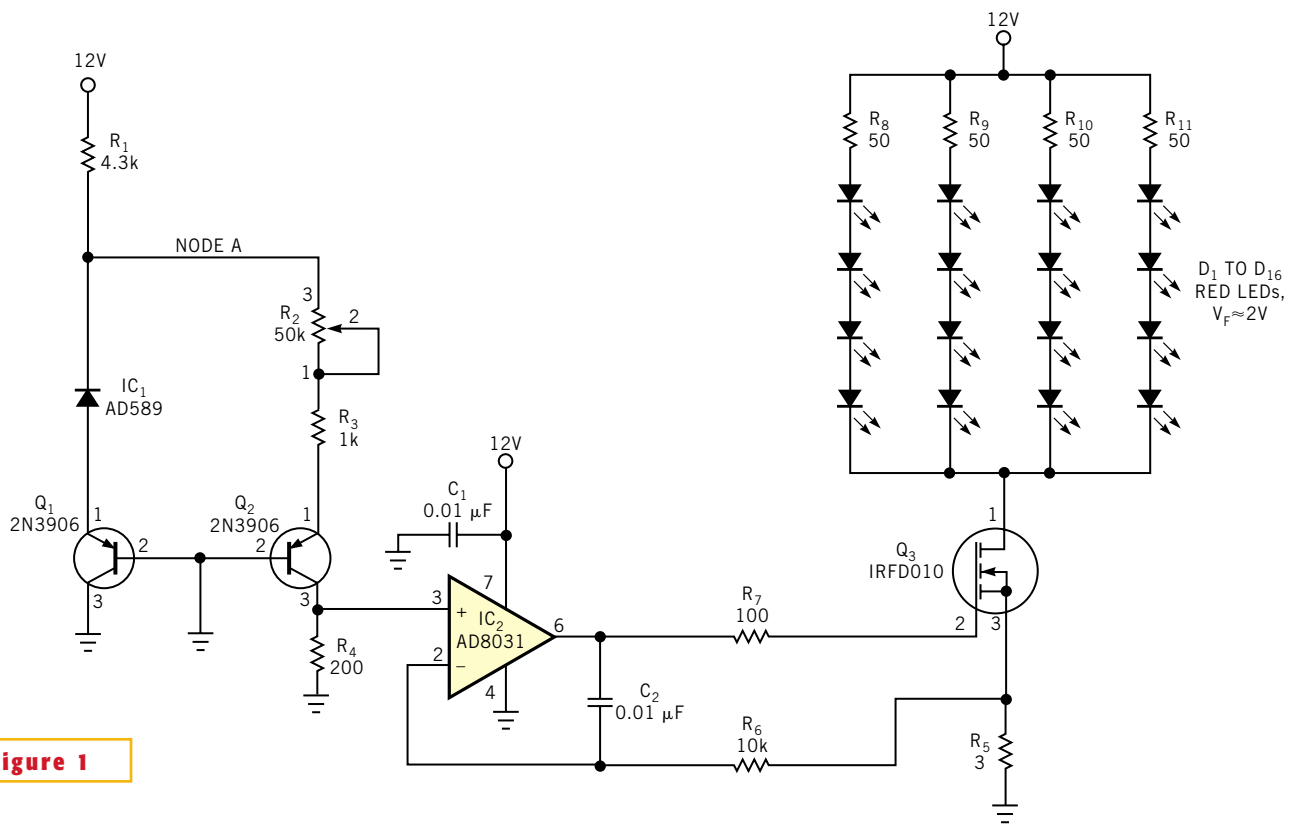

Figure 1

A handful of components provides linear adjustment of a darkroom's safe light.

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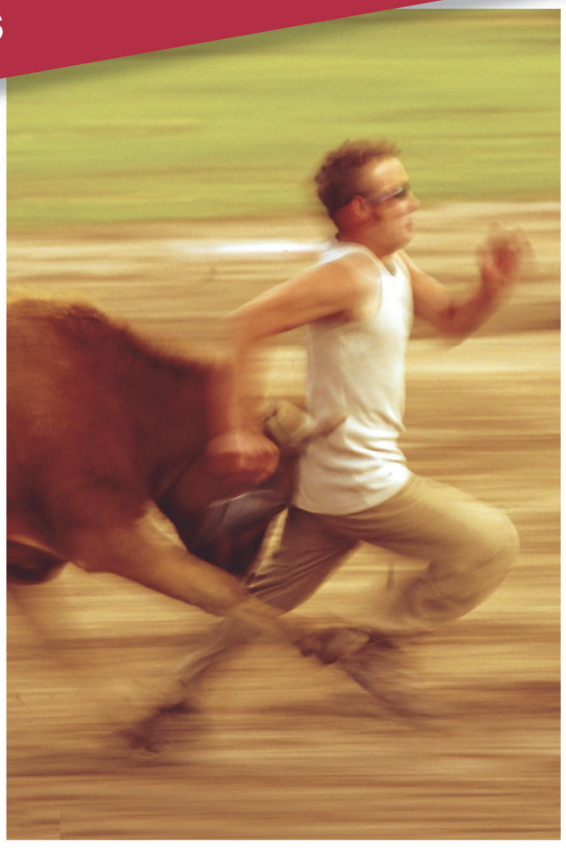
Intersil High Performance Analog



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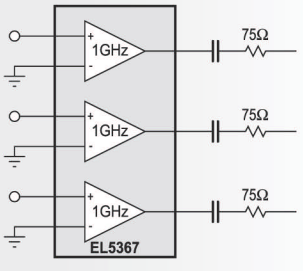

Part No.	BW (MHz)	SR (V/µs)	Is (mA)	Av (min) (V)	IOUT (mA)	VOUT (V)
EL5360	200	1700	0.75	1	70	±3.4
EL5362	500	2500	1.5	1	100	±3.6
EL5364	600	4200	3.5	1	140	±3.8
EL5367	1000	6000	8.5	1	160	±3.8

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- Less than 9mA power consumption

Part No.	# of Amps	BW (MHz)	SR (V/µs)	Is (mA)	Av (min) (V)	IOUT (mA)	VOUT (V)	VOS (max) (V)
EL5160/1	1	200	1700	0.75	1	70	±3.4	5
EL5162/3	1	500	4000	1.5	1	100	±3.6	5
EL5164/5	1	600	4700	3.5	1	140	±3.8	3.5
EL5166/7	1	1400	6000	8.5	1	160	±3.8	5
EL5260/1	2	200	2000	0.75	1	70	±3.4	5
EL5262/3	2	500	2500	1.5	1	100	±3.6	5
EL5462	4	500	2500	1.5	1	100	±3.6	5

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- Low power consumption

Part No.	# of Amps	BW (MHz)	SR (V/µs)	VN (nV/√ Hz)	Is (mA)	IOUT (mA)	VOUT (V)	VOS (max) (V)
EL5100/1	1	300	2200	10	2.6	100	±3.4	5
EL5102/3	1	400	2200	6	5.2	150	±3.7	5
EL5104/5	1	700	4500	14	9.5	160	±3.8	5
EL5202/3	2	400	2200	6	5.2	150	±3.9	5
EL5204/5	2	700	3000	10	9.5	160	±3.8	10
EL5300	3	200	2200	10	2.5	100	±3.4	4
EL5302	3	400	2200	6	5.2	150	±3.7	5
EL5304	3	700	3000	10	9.5	160	±3.8	10

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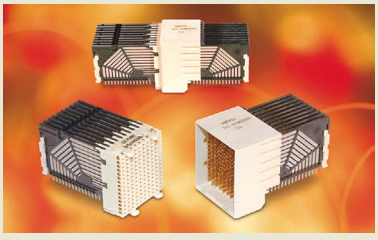


Coplanar connector has low insertion loss and crosstalk

AirMax VS system's coplanar version allows for insertion of add-in boards for system upgrades. The system uses air as the dielectric between adjacent conductors, facilitating high signal density and exhibiting low insertion loss and crosstalk. The product allows designers to freely mix as many as 63 differential-pair lines per inch, as many as 95 single-ended signals per inch, and a power supply in one connector. The high-density, 25-mm card slot also includes a two-piece header-receptacle connector system in 3- and 2-mm column spacing in a 150-position, five-pair configuration for 25-mm-slot-pitch applications and a 120-pitch, four-pair connector for 20-mm-slot-pitch applications. The coplanar connector cost 10 cents per mated line.
FCI, 1-800-237-2374, www.fciconnect.com

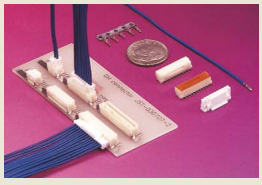
Adapter has carrier-class connectivity for European-sourced DS3/video products

The UADF20M110 adapter couples a 1.6/5.6 DIN plug to a full BNC jack and delivers true 75Ω performance. The adapter enables connectivity of European-sourced products to DS3 telephone-company-network and video-broadcast applications in the North American conventional footprint. $40.80 (100).
Trompeter, 1-800-982-2629, www.trompeter.com

BMI connector has self-aligning feature

The Spox BMI (blind-mate-interface) connectors have a self-aligning feature for a lower installation time and expanding design options in wire-to-board and wire-to-wire applications. The low profile allows for a mated stack distance of 11 mm. The dual-row, panel-mount design on a 2.5-mm centerline provides support for BMI applications and supports as much as 3 mm of horizontal and vertical misalignment between connectors before engagement. The connectors come in wire gauges as large as #22 AWG for 3A current at 250V. The six-position wire-to-board mated connector costs 70 cents in high volumes.
Molex Inc, www.molex.com

Connector suits critical high-density applications



The 1.25-mm-pitch, top- and side-entry wire-to-board GH Series SMT connectors feature positive locking, including audible-click/tactile feedback, when mating to headers. The connector is available with two to 15 circuits rated 1A ac/dc AWG #26 at 50V ac/dc; it accommodates wire sizes AWG #30 to #26.
JST Corp, 1-800-947-1110, www.jst.com

Microprocessors

SOCs have touchscreens and programmable LCD controllers

The 16/32-bit LH79525 and 32-bit LH79524 SOCs (systems on chips) include an on-chip, programmable, color LCD controller, an onboard 10/100BaseT Ethernet MAC (media-access controller), USB functions, serial ports, and external DMA. The LCD controller supports 65,536 colors in the LH79524 and 4096 colors in the LH79525, and both SOCs feature a direct interface to STN (supertwist-neumatic), color STN, TFT (thin-film-transistor), and Sharp's Advanced-TFT panels. The products' peripherals include16 kbytes of on-chip SRAM, I²C, I²S, counter/timers, an SDRAM controller, and a watchdog timer, as well as all types of flash memory. The LH79524 comes in a CABGA-208, and the LH79525 comes in an LQFP-176. Both components will be available in mass-production quantities early in the second quarter of this year.
Sharp Microelectronics of the Americas, www.sharpsma.com

JPEG compression suits FPGA-based intelligent cameras

The high performance CTJPEG-04 JPEG-compression IP (intellectual-property) core suits FPGA-based intelligent cameras. The core can sustain 500 frames/sec at a resolution of 1280×1024 pixels. Based on the JPEG ISO/IEC IS 110917-1 standard image-compression algorithm, the core uses a configurable user interface to compress images from FastVision's cameras and then transmits the images to a host through a USB-2-standard interface. The core is synchronous and autonomous, and it features localized graceful image degradation. Input to the core comes from a Micron Imaging-type sensor at a pixel rate of 10 pixels of 10 bits on every cycle of a 66-MHz clock. The core frequency-transforms samples using a discrete cosine

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Microprocessors

transform with an 18-bit internal accuracy and feeds them through one of two Huffman and quantization tables, which are configurable during compression. The core outputs JPEG-JFIF- or motion-JPEG-compressed data that users can convert back to standard image formats. The product requires no external memory, suits Xilinx Virtex XC2V2000 FPGAs, and is available in configurations accepting a variable number of pixels per cycle and pixel resolution.
Cadre Codesign Inc, www.cadrecodesign.com

Third-party vendor provides real-time OS support

Enea's OSE RTOS provides real-time operating-system support for Texas Instruments' C64x DSP, as well as all previous-generation C64x DSPs in both single-processor and multiprocessor configurations. The OSE provides interprocessor-communications mechanisms that allow multiple processes running on multiple DSPs to communicate as though they were on the same DSP.
Enea Embedded Technology, www.enea.com

Electronic Design Automation

ISE plugs directly into EDA design flows

The ISE (integrated software environment) 7.1i integrates key power-analysis, hierarchical-design, simulation, and debugging features and supports Linux-based design environments. The ISE features a design-summary view and message filtering, highlighting important design information. A technology viewer displays postsynthesis-implementation results in a schematic view. The product also includes the ISE simulator and ModelSim Xilinx Edition-III; ChipScope Pro, providing remote system debugging; and the ability to directly plug into EDA design flows, including deep integration to third-party EDA-partner design tools. The product integrates with the vendor's PlanAhead option, allowing a new layer of hierarchical design and decreasing design cycles with incremental compiling, fewer timing iterations, and efficient intellectual-property planning and reuse. The ISE 7.1i suits the company's Virtex-4 and Spartan-3e FPGA families and supports 64-bit Linux. Prices range from $695 to $2495.
Xilinx Inc, www.xilinx.com

Programmable bridge targets use in Intel PXA2XX

QuickLogic Corp has announced its first product in a series of uWatt programmable bridges for Intel PXA2XX processor line, which QuickLogic based on the Intel XScale microarchitecture. The QuickPCI-based bridge allows designers to expand the Intel XScale microarchitecture's native peripheral set to communicate with PCI-based peripherals, such as Wi-Fi, Ultra Wideband, and USB 2.0 to aid users targeting application such as handheld GPS, portable medical systems, voice-over-wireless-LAN PDAs, and smart phones. In addition to the bridge, QuickLogic has developed a Wi-Fi product comprising a daughtercard that plugs into Intel's PXA270-based mainstone processor developer's kit using a VLIO (Variable Latency I/O) connector and a Linux OS board-support package. QuickLogic plans to support the Windows CE and Windows Mobile operating systems over the coming months.
QuickLogic Corp, www.quicklogic.com

Upgrade automatically reads and checks SDC

Chip2Nite Version 2.1's upgrade allows for automated reading and checking of SDCs (Synopsys design-constraints) files, enabling logic designers to verify the files early in the design process, reducing overall design-cycle time. The product includes automatic macro placement and block floorplanning capabilities, as well as support for groups and floorplans, allowing designers to classify logic into groups and assign them to regions of the floorplan; postplacement-analysis features, such as pin density to reduce congestion and to support top-level pins; and five to 10 times speed and capacity improvements over typical-database loading times, which are critical to performing rapid prototyping and what-if analyses.
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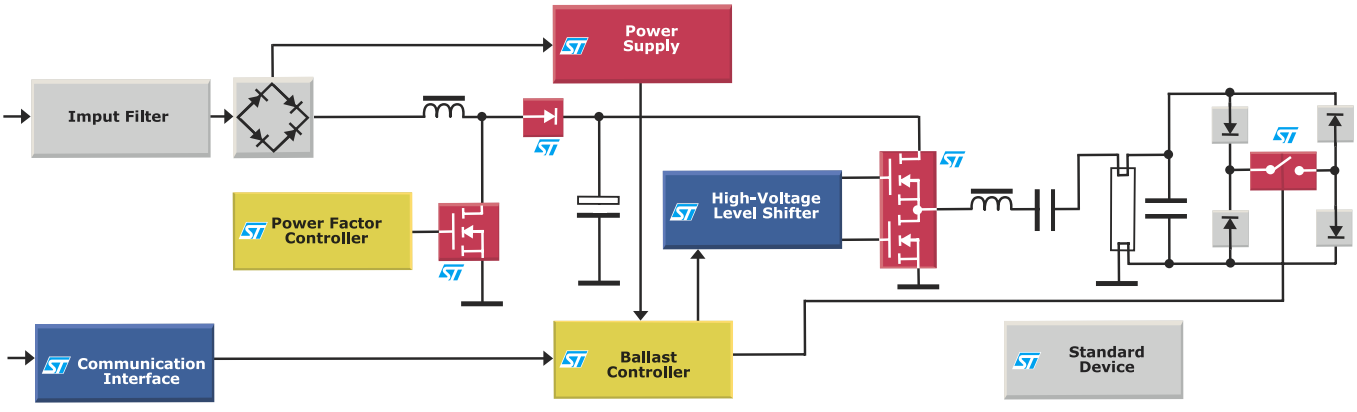

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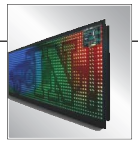
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